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Static Induction Devices with Planar Type Buried Gate

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Abstract: Based on the surface-gate and buried-gate structures, a novel buried-gate structure called the planar type buried-gate (PTBG) structure for static induction devices (SIDs) is proposed. An approach to realize a buried-gate type static induction transistor by conventional planar process technology is presented. Using this structure, it is successfully avoided the second epitaxy with a high degree of difficulty and the complicated mesa process in conventional buried gate. The experimental results demonstrate that this structure is desirable for application in power SIDs. Its advantages are high breakdown voltage and blocking gain.

Key words: static induction device; planar type buried gate structure; blocking voltage; limiting field ring
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1 Introduction

In recent years, scientists and researchers have been greatly interested in static induction transistor (SIT) due to its advantages[1~5] such as the high breakdown voltage, the negative temperature coefficient, the low distortion, and the low noise performances. According to the pattern of structures, SITs usually have three basic structural types: surface gate, buried gate, and recessed gate. Although it has low gate-source capacitance and high operating frequency, the surface-gate SIT in which source and gate stripes are alternately arranged on the same plane needs local oxidation and self-aligning processes. The rather low gate-source breakdown voltage is the fatal shortcoming of this structure type. The buried-gate SIT, in which the gate stripes are buried under the epitaxial layer in the channel, requires second epitaxy and mesa-etching technologies. In addition, vapor phase epitaxy usually results in the self-doping effect. Although it has high power capability, the operating frequency of the buried-gate SIT is relatively low. The recessed-gate SIT[6~8], in which gate stripes are placed in the bottom surface of a recessed or grooved region formed by etching, is developed to further reduce gate-drain capacitance due to the exist of an insulating layer under the gate region. In spite of high operating frequency and high power, the recessed-gate structure has seldom been used in technological practice because of the high degree of technological difficulty.

In this paper, we propose a novel structure type of static induction device (SID), referred to as a planar type buried-gate (PTBG) structure. In the PTBG structure, the gate region and the contacting region of the gate electrodes are formed using boron diffusion, and the source region is produced by phosphorus diffusion instead of second or source epitaxy of the conventional buried-gate structure. This new structure type not only has good high-frequency performance of the surface-gate structure, but also the high power capability of the buried-gate structure. The buried-gate structure is realized by the conventional planar process.

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SITs, as well as bipolar static induction transistor (BSIT) and static induction thyristors (SITHs) fabricated using this structure have typical I-V characteristics and satisfactory electrical performances.

2 Structure and fabrication

In order to improve the voltage performance, the entire geometrical pattern of the SID with the PTBG structure is surrounded by two p^+ limiting field rings and one n^+ surface channel stopper ring. A schematic top view is shown in Fig. 4. The source and the gate electrodes are placed on the wafer surface connected directly to the Ohmic contact region with high doping density, and the drain electrode is located at the back of the wafer, which is beneficial for increasing blocking voltage and reducing on-state voltage drop. The gate electrode is directly marked in Fig. 4, whereas the source electrode is not marked because the source region is produced by phosphorous diffusion on a large area after the gate body is formed. The source electrode is then formed using aluminum sputtering and etching. A unit of the PTBG structure, together with surface-gate and conventional buried-gate structures for comparison is schematically illustrated as a cross-section in Fig. 1. Although the schematic cross-sectional view of the PTBG structure is analogous to that of the conventional buried-gate structure, and they are different in nature. The source region of the conventional buried-gate structure is formed by second epitaxy or source epitaxy, whereas the PTBG structure is

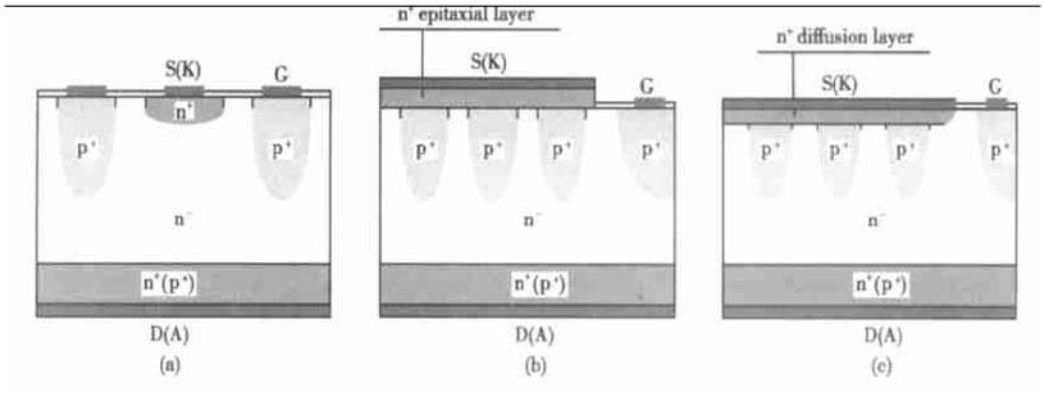

Fig. 1　Schematic cross-section of three structures　(a) SG; (b) BG; (c) PTBG

produced using phosphorus diffusion on a large area. The main structural parameters are as follows: gate-to-gate spacing $d = 2a = 16\mu m$; gate-to-drain spacing $l_{gd} = 180\mu m$; wafer thickness $300\mu m$; channel length $l_c = 10 \sim 11\mu m$; the source depth l_s varying within the range of $1 \sim 1.5\mu m$; gate thickness $d_g = 6\mu m$, channel number $N_c = 814$; total channel width $w = 1.63 \times 10^5 \mu m$; total channel area $A_c = 5.2 \times 10^{-3} cm^2$.

In order to demonstrate the general applicability of the PTBG structure, a SITH has been fabricated using an n-type Si single-crystal epitaxial wafer with 80~ 100Ω · cm resistivity, and a BSIT has been fabricated using a Si-Si direct bonding (SDB) wafer with 120~ 180Ω · cm. Like other structure types of semiconductor power devices, the fabrication of SIDs requires a high resistive layer formed on the low resistive substrate so as to achieve high breakdown voltage and low on-state resistance. At present, the conventional method to fabricate this high resistive layer on a low resistive substrate is mainly the thick epitaxy technique. This process, conducted at high temperature for a long time, can result in regenerated defects and doping redistribution, and also self-doping. Here we use SDB wafers to fabricate a BSIT with a PTBG structure. A high resistive wafer is directly bonded on to the low resistive wafer at above

1000℃ for only a short time. The thickness and surface state of the high resistive layer are determined by mature grinding and polishing technologies. The main steps for process of the PTBG structure are as follows.

(1) The NTD-Si (111) single-crystal wafer with a doping phosphorus concentration of 4×10^{13} cm^{-3} and SDB wafers with a doping concentration of $3\times10^{13}\sim 1\times10^{14}cm^{-3}$ were used as the original wafers.

(2) Boron atoms with high density were diffused into the original wafer at 1250℃, and the diffused depth was about 120μm (necessary for the fabrication of SITH).

(3) After diffusion, the wafers were ground and polished on one side, and the final thickness was controlled to be equal or shorter than 300μm.

(4) The wafers are chemically etched in HF∶HNO_3∶HAC= 1∶8∶1 at 45℃ for 30~ 50s before the processes began.

(5) An SiO_2 layer, about 600nm, was grown on the wafer, and the photoresist pattern was determined by the first masking. The SiO_2 layer was selectively etched for the gate stripes and limiting field rings.

(6) p^+ gate stripes and limiting field rings were simultaneously formed by boron deposition and driving into the wafer at 1200℃ for 4~ 6h. The diffusion depth was about 10~ 12μm, and the sheet resistance $R_\square$ was about 30 ~ 40Ω/□. The thin SiO_2 film was grown on the gate stripes and limiting field rings.

(7) The windows of source region and photoresist pattern of the channel stopper ring were determined by the second masking.

(8) The source region and channel stopper ring were coincidently formed by phosphorus diffusion on large area at 1150℃ for 20~ 45min. The diffusion depth was about 1.5μm, and $R_\square\approx3\Omega/\square$.

(9) An SiO_2 layer, about 300nm, was grown for covering the whole surface of the wafer.

(10) The metallization windows for the source and gate electrodes, the first limiting field ring as well as channel stopper ring were opened by selective etching.

(11) The metallization of drain electrodes is realized by sputtering Ni on the back of wafer, and the Al-Ti-Pt metal electrodes of source, gate, first limiting field ring and channel stopper ring were accomplished by evaporation and sputtering.

3 *I-V* characteristics of SID with PTBG structure

A SID with PTBG structure can operate in both forward conducting state and forward blocking state. In other words, not only positive but also negative gate bias voltages can be applied. In addition, static induction devices fabricated with a PTBG structure can operate in a normally-on state, and in a normally-off state as well. The various types of static induction devices are different in *I-V* characteristics and in electrical performances by the virtue of distinct parameters of structure, material, and technology, along with different biased conditions. The *I-V* characteristics of a PTBG SID operating in forward mode are discussed in this section, in which positive high voltage is biased to drain electrode D and zero voltage to source S. and the G electrode can be biased negatively ($V_G<0$) or positively ($V_G>0$).

3.1 Negative gate voltage

When $V_G<0$, the potential barrier for majority carriers is formed in the channel region near the source terminal, and the *I-V* characteristics of devices are modulated by the potential barrier, which is controlled by gate voltage V_G. As for the normally-on SIT with a PTBG structure, *I-V* characteristics of triode-like type or mixed type of pentode-like and triode-like are observed as shown in Figs. 2(a) and (b). For a normally-off type BSIT in blocking-state, triode-like *I-V* characteristics (but with a displacement along the voltage axis) are observed in small current regime as shown in Fig. 2(c). Similarly, the same situations are observed for

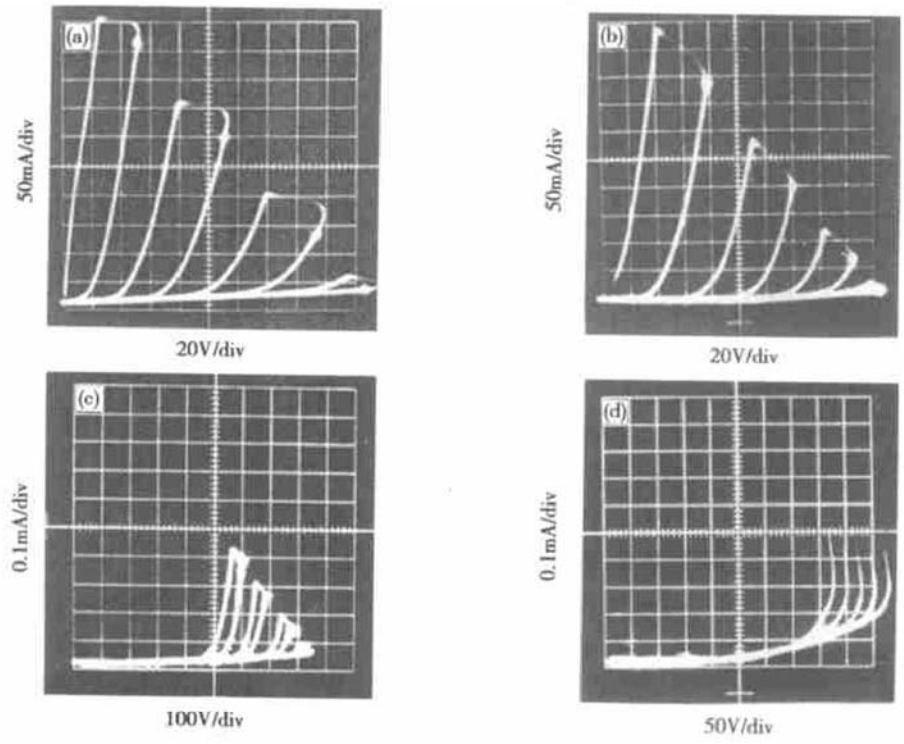

Fig. 2　Observed I-V characteristics of SID($V_G < 0$)　(a) Mixed I-V characteristics of normally-on SIT; (b) Triode-like I-V characteristics of normally-on SIT; (c) Displaced triode-like I-V characteristics of normally-off BSIT; (d) Displaced triode-like I-V characteristics of normally-off SITH

a normally-off type SITH in blocking-state as illustrated in Fig. 2(d). The behavior of the I-V characteristics of SIT with PTBG structure is identical to that of typical surface-gate or conventional buried-gate structures.

3.2 Positive gate voltage

The normally-off type BSIT and SITH mainly operate at positive gate biased voltage. When $V_G > 0.5$V, the devices are controlled by the injected minority carrier current. The approximately saturate pentode-like I-V characteristics of the BSIT are observed as indicated in Fig. 3(a). In the SITH, electron-hole plasma of double injected carriers is formed in the channel as well as the shift region, and the remarkable effect of conductance modulation occurs. At this time, the devices are operating in conducting state, similar to the behavior of a p-i-n rectifier. The observed conducting I-V characteristics are shown in Fig. 3(b). On the basis of the above discussion, it is reasonable to consider the PTBG structure as a fundamental structure for fabricating SITs.

4　Features of planar type buried-gate structure

Being noticed that the I-V characteristics of a SIT with PTBG structure have the identical fundamental features of the surface-gate and the buried-gate structures. It is necessary to illustrate some traits of them.

First, when the gate-channel p-n junction of the surface-gate structure is forward biased at $V_G > 0$, the minority carriers are injected into the channel region and accumulated; at the same time, the electrons are also injected into the channel. Therefore, there is a small recombination of current in the gate-source loop. For the PTBG structure, the gate-channel and gate-source p-n junctions are both forward biased; the holes from gate region are injected into the channel region, and also

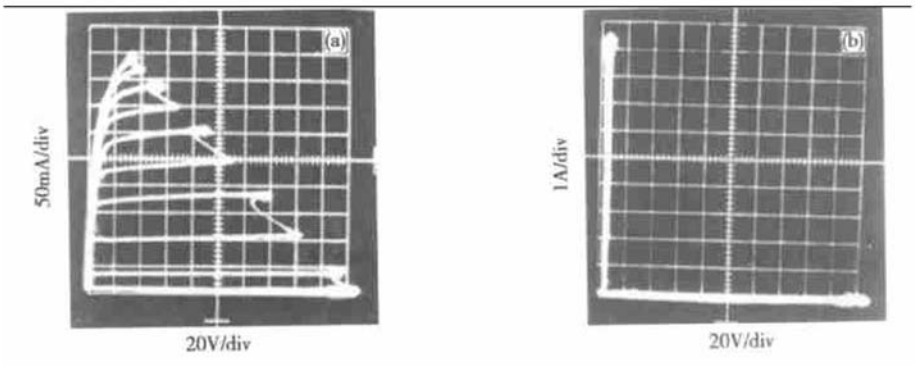

Fig. 3 Observed I-V characteristics of SID($V_G > 0$) (a) Saturated pentode-like I-V characteristics of normally-off BSIT; (b) P-i-n type I-V characteristics of normally-off SITH

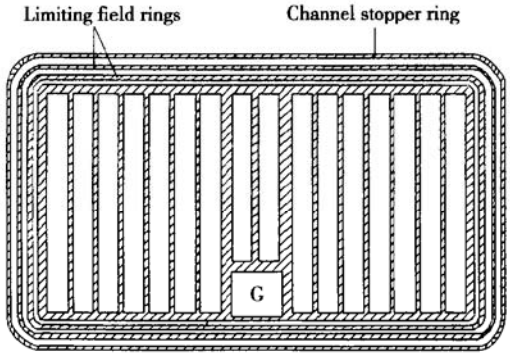

Fig. 4 Layout diagram of a BSIT with PTBG structure

into the source region. Correspondingly, there is a rather large current in the gate-source loop. Secondly, the source region of the conventional buried-gate structure is formed by second epitaxy, whereas the PTBG structure is formed by phosphorus diffusion on a large area, resulting in an impurity compensation of boron and phosphorus in the gate diffusion region, which is desirable for increasing the gate-source breakdown voltage. Thirdly, since the source phosphorus diffused region has certain depth X_{jp}, and the gate diffusion layer is a sub-diffused layer with comparatively large sheet resistance, the doping concentration of the gate region is reduced and thereby the resistivity of this region is increased. As for the large depth X_{jp}($\geqslant 5\mu$m), the gate-source p-n junction further approaches the graded transition junction, which is favorable for raising the gate-source breakdown voltage, and is convenient for turning off the device. Next, compared with the surface-gate structure, the frequency characteristics of the PTBG structure are slightly low, as a result of the large area of gate-source p-n junction. In short, the PTBG structure not only has the common features of SIDs, but also has distinctive characteristics. Different PTBG structures can be chosen according to various requirements.

5 Results and discussion

The I-V characteristics of the SITH with a PTBG structure fabricated using n-Si single-crystal wafer are illustrated in Fig. 2(d) and Fig. 3(b), and its typical electrical parameters are listed in Table 1.

Table 1 Parameters of SITH with PTBG structure

Parameter	Value
Forward blocking voltage, V_{AK}	600~ 1000V
Gate-source breakdown voltage, BV_{GSO}	8~ 10V
Gate-drain breakdown voltage, BV_{GDO}	600~ 1000V
On-state voltage drop, V_{on}	< 0.6V
Maximum drain current, I_{AM}	50A
Blocking gain, G	40~ 60
Turning-on time, t_{on}	0.2~ 0.4μs
Turning-off time, t_{off}	0.4~ 0.8μs

The typical I-V characteristics of the BSIT with a PTBG structure at forward and reverse biased gate voltage fabricated using Si-Si direct bonding wafer are shown in Fig. 2(c) and Fig. 3(a). The parameters of electrical performance are summarized in Table 2.

Table 2 Electrical performance parameters of BSIT with PTBG structure

Parameter	Value
Gate-source breakdown voltage, BV_{GSO}	7~ 10V
Gate-drain breakdown voltage, BV_{GDO}	500~ 1280V
Current amplifying coefficient, h_{FS}	≥20
Saturating voltage drop, V_{DSS}	≤0.85
Maximum drain current, I_{DM}	2A
Turning-on time, t_{on}	0.2μs
Turning-off time, t_{off}	0.4μs

The turning-off time, t_{off}, is an important dynamic parameter indicating the frequency performance of the device. The measured turning-off time t_{off}= 0.4~ 0.8μs, as listed in Tables 1 and 2, shows that the frequency of the BSIT or SITH with PTBG structure is higher than 1MHz. The excellent waveform of turning time of the BSIT with PTBG structure, as shown in Fig. 5, demonstrates superior radio-frequency behavior. Compared with a conventional buried-gate structure, the BSIT with a PTBG structure has many advantages such as a high breakdown voltage of 1280V, a large current density capability of 800~ 1000A/cm^2, a low saturating voltage drop of 0.85V and good uniformity.

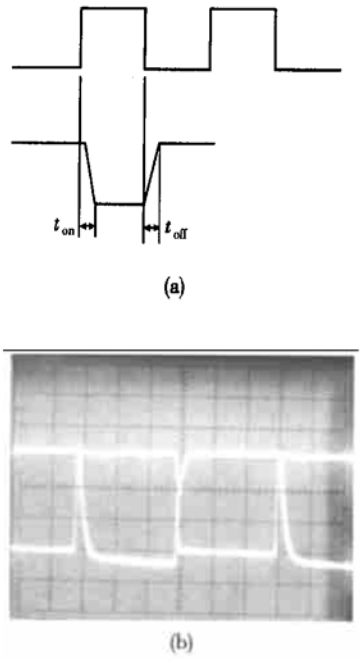

Fig. 5 (a) Schematic diagram of turning time; (b) Observed waveform of turning time of a BSIT

6 Conclusion

It has been experimentally demonstrated that the PTBG is a promising structure pattern for fabricating various static induction transistors, especially for high power devices. The simple technical process is the main merit of the PTBG structure. As long as the parameters of boron diffusion in the gate region and phosphorus diffusion in the source region are approximately matched, high breakdown voltage and high blocking gain can be easily obeained.

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平面型埋栅结构的静电感应晶体管

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摘要: 在表面栅和埋栅结构的基础上,提出了一种制造静电感应晶体管的新型结构,平面型埋栅结构. 用普通的平面工艺实现了具有高击穿电压的埋栅结构,避免了工艺难度较大的二次外延和台面腐蚀工艺. 实验结果表明该结构可用于制造各种功率静电感应器件,其优点是具有高的击穿电压和高的阻断增益,并讨论了平面型埋栅结构的主要特点和制造工艺.

关键词: 静电感应晶体管; 平面型埋栅结构; 阻断电压; 限场环

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