第 25 卷第 2 期 半 导 体 学 报 Vol. 25, No. 2
2004 年 2 月 CHINESE JOURNAL OF SEMICONDUCTORS Feb., 2004

Co-Design of Monolithically Integrated Photo-Detector and Optical-Receiver*

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Abstract: A behavioral model of the photodiode is presented. The model describes the relationship between photocurrent and incident optical power, and it also illustrates the impact of the reverse bias to the variation of the junction capacitance. According to this model, the photodiode and a CMOS receiver circuit are simulated and designed simultaneously under a universal circuit simulation environment.

Key words: monolithically integrated; co-design; behavioral model
EEACC: 4250; 2560B
CLC number: TN303 **Document code**: A **Article ID**: 0253-4177(2004)02-0133-05

1 Introduction

It has been shown that monolithic OEIC (optoelectronic integrated circuit) can eliminate some parasitic effect caused by wire-banding between optoelectronic device and Si-based signal processing circuit, thus increases the band-width of the optoelectronic system. Several works about this have been reported in these years[1~3]. But the photo-detector and the receiver were designed separately in previous researches, so the performance of integrated system would not be optimized jointly[1~3]. It is also difficult for designers to identify the general characters of the optoelectronic system. In order to accomplish a comprehensive simulation for OEIC in one developing environment, we develop an analog behavioral model of the PIN photo-detector. According to this model, some information such as the maximal band-width and the sensitivity under a given incident optical power can be achieved.

2 Analog behavioral model of photo-detector

To construct circuit models of optoelectronic devices, we should employ some components in EDA system to express their electronic characters. Dependent sources, which are available in all circuit simulation software, are originally used to establish circuit macro models. But we have to ignore their meanings of electronics, and only take their computing ability into consideration. Various theoretical equations in optoelectronics can be represented by electronic device via this way.

* Project supported by National High Technology Research and Development Program of China (Nos. 2001AA312080, 2001AA122032, and 2002AA312240)

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Received 12 June 2003, revised manuscript received 6 August 2003

The cross-section of a CMOS technology-compatible interdigitated structure photodiode and its equivalent circuit are presented in Fig. 1[4].

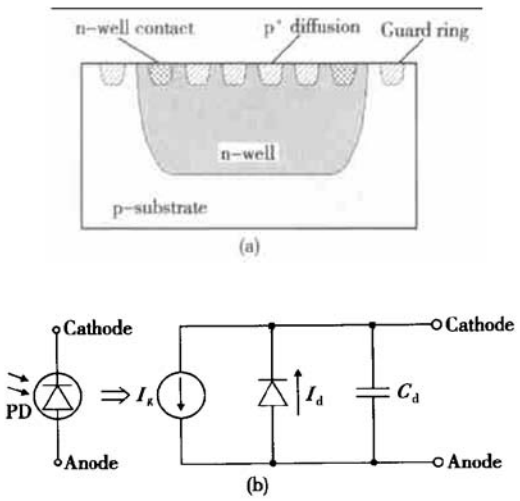

Fig. 1 (a) Schematic cross-section of photodiode; (b) Equivalent circuit of photodiode

2.1 Photo-generated current

In Fig. 1 (b), the current source I_g is introduced to simulate the photo-generated current. The relationship between I_g and incident optical power P_{opt} can be easily obtained as

$$I_g = RP_{opt} \tag{1}$$

$$R = \frac{I_g}{P_{opt}} = \eta \frac{q\lambda}{hc} \tag{2}$$

$$\eta = (1 - P_{ref})e^{-\alpha d}(1 - e^{-\alpha W}) \tag{3}$$

where R and η are defined as responsivity and quantum efficiency respectively. To construct a circuit model for the optoelectronic device, a normal DC voltage source should be employed as a virtual optical input terminal in order to simulate the P_{opt}[5].

For a given η, the responsivity increases linearly with incident optical wavelength. And the key factors determined the quantum efficiency are the absorption coefficient α and the thickness of the absorption layer W.

Since the photo-diode is fabricated under a standard CMOS process, p^+ implant in the n-well forms the pin structure here. The depleted region thus can be considered equivalent to the photon absorption layer:

$$W = \sqrt{\frac{2\epsilon_r\epsilon_0(V_D - V)}{qN_D}} \tag{4}$$

where V_D is the contact potential of the p-n junction, and V is the bias between the electrode. All the variables in the formulas (1) ~ (4), including the doping density of the n-well and the p^+ implant, can be acquired from the MOS device SPICE model parameters offered by semiconductor manufacturers.

2.2 Parasitic capacitor

The pin photodiode has a high electric field in the depleted region, which serves to separate photo-generated electron-hole pairs. For high speed operation, the region must be kept thin to reduce the transmitting time. On the other hand, in order to increase the quantum efficiency, the depletion layer must be thick enough to ensure as many photons to be absorbed as possible. Thus a trade-off is needed between the speed and quantum efficiency. C_d in Fig. 1 represents the parasitic capacitance of the photodiode. Because the photo-diode works at reverse bias, the diffusion capacitance can be ignored. It can be simply calculated as

$$C_d = \epsilon_r\epsilon_0 \frac{A}{W} \tag{5}$$

Since the dielectric layer thickness W is modulated by the potential values between the electrodes, we can construct a behavioral model of the variable capacitor as shown in the figure below.

From the model described in Fig. 2, the I-V character of a capacitor can be extracted out easily as

$$I_c = C_d \frac{dV_{cap}}{dt} \tag{6}$$

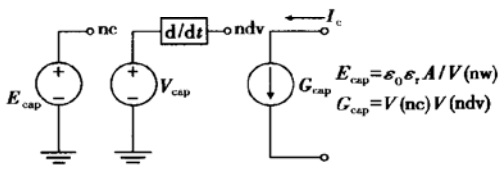

Fig. 2 Behavioral model of variable capacitor

2.3 Diode

The diode in Fig. 1 is used to simulate the reverse leakage current. We can use a normal diode device SPICE model in stead of it.

In brief, the circuit model of the photodiode has been constructed (shown in Fig. 3). All the essential elements can be acquired in a normal circuit simulation process. So the photodiode model can be connected to the receiver circuit seamlessly and be simulated simultaneously.

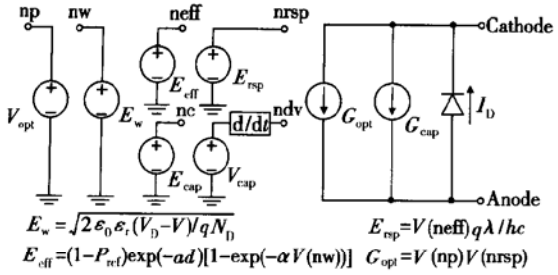

Fig. 3　Behavioral model of photodiode

3 CMOS circuit design

An example of CMOS-based optical receiver circuit is shown in Fig. 4, which consists of 3 stages.

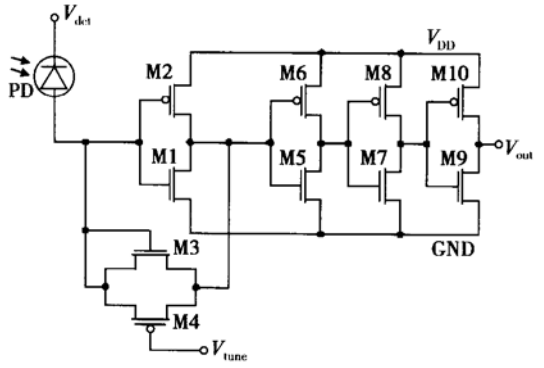

Fig. 4　Schematic of optical receiver circuit

The first stage (M1~ M4 in Fig. 4) is an inverter-based transimpedance amplifier (TIA) with a p-type FET (M4) as the feedback element. The gate voltage (V_{tune}) of this device can be adjusted for optimum performance at a given bit rate and optical power. In parallel with M4, a diode-connected n-type FET (M3) is added in the feedback loop. This element can provide some dynamic range improvements by reducing the effective feedback resistance at high incident optical power[2]. The second stage (M5, M6 in Fig. 4) functions as the voltage gain amplifier, and the last stage (M7~ M10 in Fig. 4) acts as an asynchronous discriminate circuit, which transmits and transforms the analog signal to a logic-level output.

4 Simulation result and analysis

The monolithically integrated OEIC is realized in CSMC-HJ 0.6μm CMOS process through ICC. The device model offered by the foundry is BSIM3 V3 version, from which we can get all the important parameters for establishing the behavioral model of the photodiode. Under the Avant! Hspice circuit design environment, some simulations are done as below.

4.1 Sensitivity design

The sensitivity of an optical receiver is the minimum incident optical power required for a given BER (bit error rate). In short, we can also define the sensitivity to the incident optical power while the signal transition occurs at the output terminal of the receiver.

In Fig. 5, the variation of the sensitivity at different V_{tune} is shown. From this figure, it can be seen that the sensitivity descends along with the increasing of the potential applied to the gate of M4 (Fig. 4).

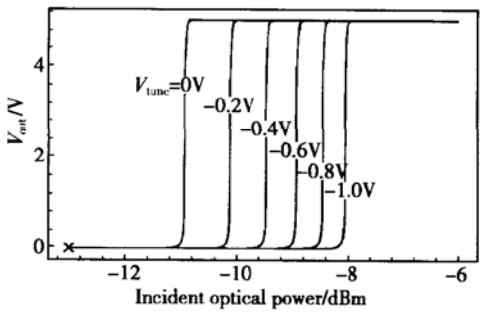

Fig. 5　Variation of sensitivity at different V_{tune}

4.2 Bandwidth design

With the - 3dB bandwidth, we can approximatively estimate the bit rate of the receiver via the relation BitRate= Bandwidth × 1.4. Frequency response at the output node of the transimpedance amplifier is illustrated in Fig. 6. Opposite to the sensitivity, the bandwidth changes in the identical direction with V_{tune}.

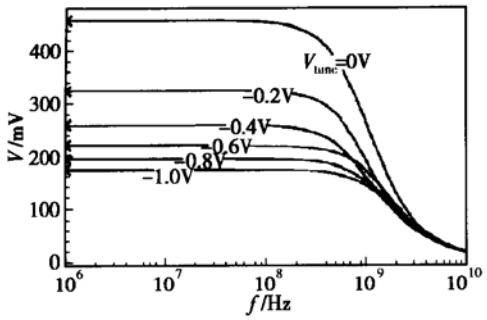

Fig. 6 Variation of - 3dB bandwidth at different V_{tune}

In the receiver circuit (Fig. 4), the available transimpedance gain (G_t) at low frequency is given as

$$G_t = \frac{-R_f}{1+1/A} \tag{7}$$

and available - 3dB bandwidth is given as

$$f_{-3dB} = \frac{A+1}{2\pi R_f C_T} \tag{8}$$

where R_f is the resistance of the feedback element, A represents the open-loop gain of the inverter-based amplifier and C_T is the total capacitance at the input node of the circuit. Equations (7) and (8) indicate that there is a trade-off between G_t and f_{-3dB}. It also means that a trade-off exists between sensitivity and bandwidth.

As the equivalent feedback resistance is controlled by the V_{tune}, we should optimize the V_{tune} as high speed as possible with moderate sensitivity.

The simulation result is close to the result reported by Mao *et al.*[6], which was achieved in Silvaco TCAD system. So this method is a practical way to design large-scale optical-electronic systems.

This monolithic OEIC is intended to be used in VSR (very short reach) optical internetworking system, which is a 12-channel parallel transmission system at 850nm. The die photograph is give in Fig. 7.

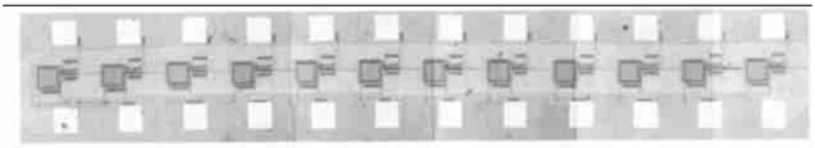

Fig. 7 Die photograph of 12-channel integrated optical receiver

5 Conclusion

We proposed a new method for designing monolithically integrated optoelectronic device and CMOS circuit. Behavioral model, which is originally intended to simplify the large scale mixed-signal simulation, gives us a way to co-simulate the optoelectronic-device and the circuit simultaneously in the same design system. We have designed an integrated optical receiver via this way, and further improvement would be achieved by modifying the structure of the photodiode and the circuit[1], or by improving the fabrication process.

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单片集成光电探测器与接收机的协同设计*

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摘要: 建立了光电探测器的行为模型. 此模型描述了注入光功率与光生电流的关系, 以及反偏电压对光生电流与结电容的影响. 给出了在统一的 SPICE 设计环境中对光电子器件与电路协同设计的方法, 并对光电探测器与 CMOS 接收机电路进行了设计.

关键词: 单片集成; 协同设计; 行为模型

EEACC: 4250; 2560B

中图分类号: TN303　　**文献标识码**: A　　**文章编号**: 0253-4177(2004)02-0133-05

* 国家高技术研究发展计划资助项目(Nos. 2001AA312080, 2001AA122032, 2002AA312240)

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2003-06-12 收到, 2003-08-06 定稿