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Design of RTD-Based TSRAM

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Abstract: A RTD-based TSRAM cell is introduced. The mechanism of different types of access transistors in this cell is described and NMOS is found most suitable from consideration of the cell size and power consumption. The architecture of a TSRAM system is presented. Simulation results show that the RTD-based TSRAM has advanced characteristics of small area, low power, and high speed.

Key words: RTD; TSRAM; high speed; low power
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1 Introduction

Tunneling-based static random access memory (TSRAM), which is based on the negative-differential-resistance (NDR) of quantum mechanical resonant current, is introduced and widely researched in recent years[1~4]. Compared with the conventional SRAM memory, TSRAM cell size is decreased greatly because it only needs one MOS transistor and two NDR devices. Furthermore, by decreasing the current density of NDR devices, TSRAM with very low standby power (50nW/bit) has also been demonstrated[2].

Owing to its good compatibility with current IC technologies, RTD is more suitable to be used in TSRAM than other NDR devices. Large scale integration (LSI) of transistor/RTD technology has been demonstrated in compound semiconductor material system[2]. Recently, Morita and Rommel described resonant interband tunneling diodes compatible with silicon-based CMOS technology[5,6]. Simulation proves[7] that silicon-based CMOS/RTD TSRAM has low power and high density appearing a promising future memory.

Area, speed, and power are key performances that we mainly concern on in design of SRAM memories. In RTD-based TSRAM, the characteristics of both the access transistor and the RTDs determine the performance of the cell. The mechanism of three different types of access transistors in the TSRAM is first described in this paper. Then, the characteristics of the nMOS-selected TSRAM are discussed and a memory system architecture is finally introduced. The Star-Hspice 2000.2 is used for simulation .

2 Selection of access transistor

Figure 1(a) shows the structure of a RTD-based TSRAM cell consisting of an access transistor and a pair of RTDs. Figure 1(b) shows the load line of the RTD pair. There are two stable points. Therefore, it is a latch, which naturally stores 1 bit.

In the following analysis, the "I_1-I_2" curve in Fig. 1(b) is used as the load line in the TSRAM cell, and I_3 (current of the access transistor) as the

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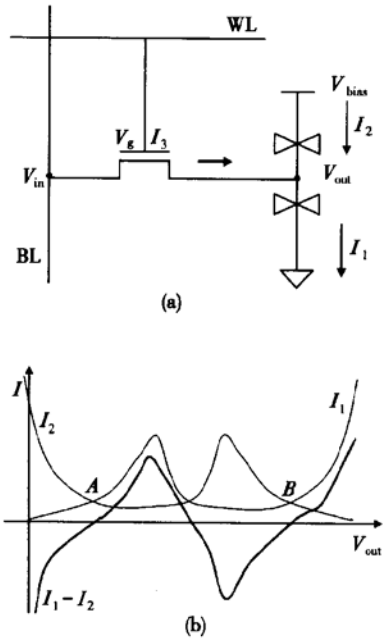

Fig. 1 (a) Schematic of a TSRAM cell; (b) Load-line diagram of the RTD latch

driving line. The access transistors are based on a 0.35μm CMOS technology. The equivalent circuit model of RTD is in Fig. 2, which includes a shunt-wound capacitor and a voltage-dependent current source connected to a resistor and an inductor in series. The simulation result shows that this model fits experiment results well. The values for the

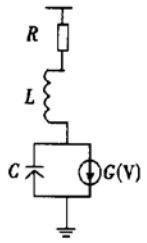

Fig. 2 Equivalent circuit model of RTD

components used in this paper are $R = 8\Omega$ for the resister, $L = 1.07 \times 10^{-11}$ H for the inductor, $C = 1.01 \times 10^{-13}$ F for the capacitor, and the current source $G(V)$ is from the physics-based RTD current-voltage equation[8]. The parameters in the equation are $A = 104$, $B = 0.035$, $C = 0.1472$, $D = 0.0052$, $n_1 = 0.115$, $H = 1.411$, $n_2 = 0.1201$. The parameters are extracted from the I-V curve of a real InGaAs/AlAs RTD. The RTD's area is $1\mu m^2$.

The driving capability of the access transistor is important to the "write" operation. Low driving current may cause malfunction. The characteristic of nMOS as the access transistor is discussed. Both V_{bias} and V_g are set to 3V, and V_{in} is stressed from 0 to 3V. The curves of V_{out} versus V_{in} with access transistors of identical channel length (0.35μm) but different widths are shown in Fig. 3(a). The load-line diagram is in Fig. 3(b). When channel width is small (1μm and 2μm), V_{out} increases from 0, the "1" curve crosses with the RTD-latch's load line at point A and the cell becomes stable temporarily. When the access transistor turns off, the stable point turns to point D. Therefore, although V_{in} is high (> 1.5V), V_{out} stays low (< 1.5V), causing a wrong "write" operation. However, the "3" curve can pass over the current peak, and crosses with the RTD-latch's load line at point C. The cell stays stable at point C, performing the "write" operation correctly.

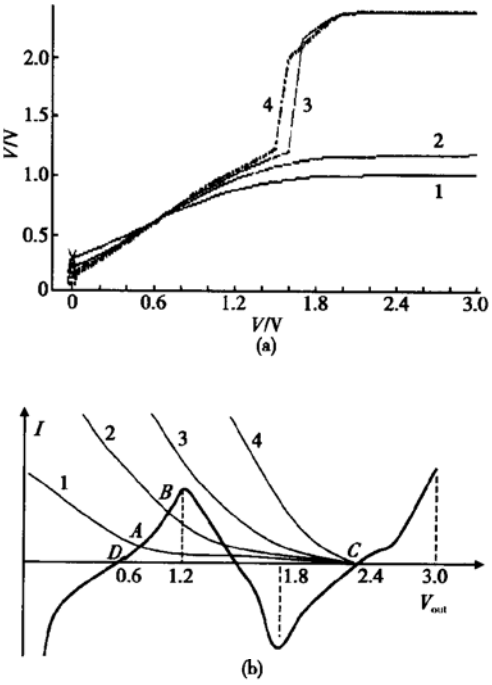

Fig. 3 (a) Conduct performance for high voltage with nMOS; (b) Load-line diagram

For comparison, the driving lines of nMOS, pMOS, and CMOS as the access transistor respectively are plotted in one picture. Figure 4(a) shows

that the access transistor with nMOS (2μm width) or pMOS (1μm width) can not perform a writing "1" operation with V_{in} = 3V. The CMOS access transistor can improve the driving capability, therefore fulfill a correct write operation. Similar situation, when V_{in} = 0, is shown in Fig. 4(b). Figure 4 demonstrates that CMOS has the strongest driving ability as the access transistor. However, CMOS has two transistors, which increas the cell size and the complexity of interconnecting.

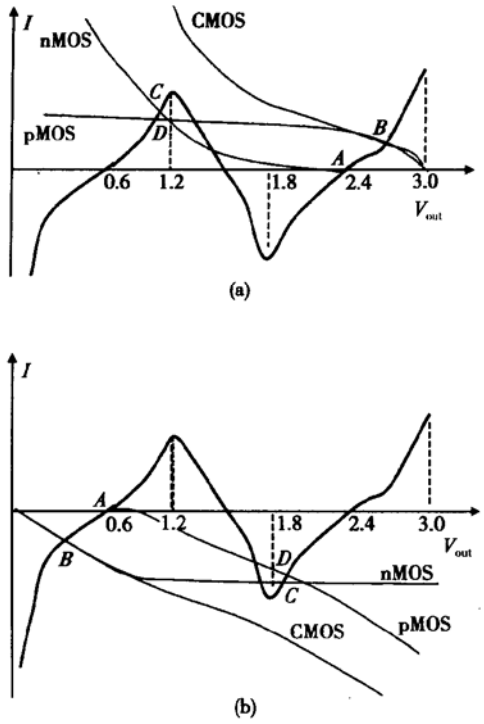

Fig. 4 (a) Load-line diagram when conducting high voltage; (b) Load-line diagram when conducting low voltage

It is found that increasing the width of nMOS enhances its driving ability greatly (see Fig. 3). Simulation results show that nMOS with 3μm width is able to write both "1" and "0" properly and allows much larger noise margin of V_{in} than the CMOS (1μm nMOS and 2μm pMOS). It also saves area compared with the CMOS. But 7μm width is needed for pMOS to write properly.

If power is considered, nMOS and pMOS have advantages under different conditions. Referring to Fig. 4(a), during the operation of writing "1", the stable point of the cell with nMOS is "A" with nearly zero current. The stable point of the cell with pMOS or CMOS is "B" with some static current. Therefore, nMOS saves power here. However, during writing "0" referring to Fig. 4(b), pMOS saves power.

From the discussion above, it is concluded that nMOS is most suitable for the access transistor in the TSRAM cell for the consideration of the cell size and power consumption.

3 Performance of the cell

The transient characteristic of the nMOS-selected TSRAM cell is shown in Fig. 5. The cell stores the input data properly with a delay of 1ns more or less. It is faster compared with other SRAM cells. According to Ref. [9], the switching time of RTD could be as short as 1.5ps. It shows that RTD-based TSRAM has great potential in ultra-fast memories.

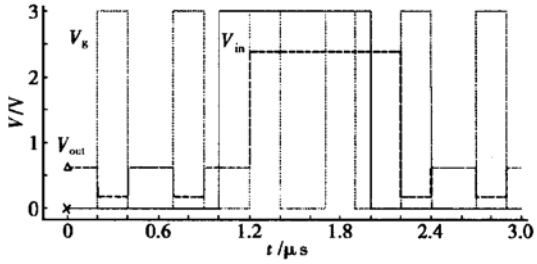

Fig. 5 Transient characteristic of the TSRAM cell

The power consumption is discussed here again. When the access transistor turns off, the static current of the RTD latch is 8.5μA (0.4μm × 0.4μm RTDs, 0.35μm long, and 0.4μm wide nMOS in the TSRAM cell). In this case, the current during writing "0" and "1" operation is 43μA and 9.3μA respectively. It is obvious that the power is still too high for utilization in memories. The main reason is that the current density of RTDs used here is 35kA/cm^2, which consumes too much current at the stable points. To decrease the power consumption, the current density of the RTD needs to be reduced inevitably. Using RTDs with current

density of 0.16A/cm^{2}[2], the static current of the TSRAM cell is reduced to the level of pA, and shows great advantage over the traditional SRAM for its ultra-low power.

The size of RTDs is important to reduce the size of the access transistor in the TSRAM cell. The width of the nMOS needs to be enlarged to 3μm to write properly when the size of RTDs is 1μm × 1μm. On the other hand, if we reduce the size of RTD to 0.4μm × 0.4μm, the width of the nMOS can be scaled to 0.7μm while not decreasing the input noise margin. The reason for this change is that with reducing the size of the RTDs, the peak of the RTD latch's I-V curve in the load-line diagram declines, and avoids crossing with the driving line of nMOS (referring to Fig. 3(b)). For the same mechanism, reducing the level of current density of RTDs permits reducing the size of the access transistor.

4 Architecture of a TSRAM system

The system architecture of a RTD-based TSRAM is shown in Fig. 6, in which some important sub-circuit modules are included, such as the memory array, word-line decoder, bit-line decoder and predecoder, read/write switch, and sense amplifier.

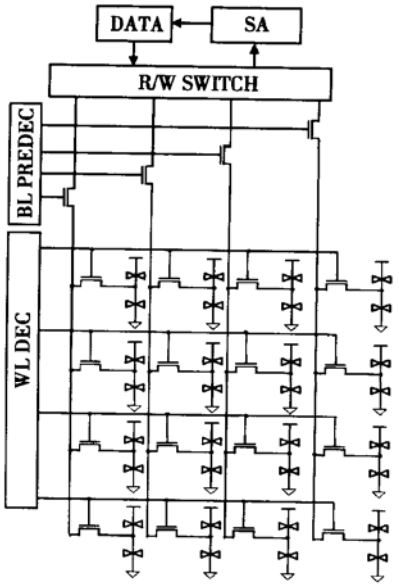

Fig. 6 Schematic of TSRAM array

This memory can be "write" and "read" with the conventional sense amplifier or QMOS sense amplifier[3].

Since RTDs are vertically integrated on the drain region of the access transistor, TSRAM cell saves area of other 5 transistors in standard 6T SRAM. Therefore, the TSRAM array has much higher density. Experiment proves that a 4×4 array of this TSRAM achieves four times higher density than that of the 6T SRAM using the same design rules[2].

5 Conclusion

The key factors determined and effected the function and performance of a RTD-based TSRAM cell are investigated in this paper. The conclusions are listed below:

(1) nMOS is most suitable to be used as the access transistor in the team of cell size and the power consumption.

(2) Too small width of the access transistor leads to improper "write" operation or worse input noise margin.

(3) With only one MOS transistor, TSRAM cell saves 70% area than the traditional 6T SRAM.

(4) Reducing the area and the current density of RTDs can save both area and power of the TSRAM cell. The static current can be reduced to pA level with proper RTDs.

(5) The delay of "write" operation is less than 1ns, which demonstrates that the RTD-based TSRAM has higher "write" speed compared with the conventional SRAM technologies.

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基于共振隧穿二极管的 TSRAM 设计

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摘要: 介绍了基于共振隧穿二极管的隧穿静态随机存储器的单元结构和原理. 讨论了 nMOS, pMOS 和 CMOS 作为单元里的选中管的特点, 综合考虑面积和功耗后, 发现 nMOS 是选中管的最佳选择. 设计了基于 RTD 的 TSRAM 系统结构. 模拟显示了这种新型存储器具有高集成度、高速和低功耗的优势.

关键词: 共振隧穿二极管; 隧穿静态随机存储器; 高速; 低功耗

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