ISM Band Medium Power Amplifier*

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Abstract: With the large-signal model extracted from the InGaP/GaAs HBT with three fingers, a three-stage, class AB power amplifier at ISM band is designed. Through the optimization of the traditional bias network, the gain compression at the low input power level is eliminated successfully. At 3.5V of supply voltage of the power amplifier after optimization exhibits 30dBm of maximum linear output power, 43.4% of power added efficiency 109.7mA of a quite low quiescent bias current, 29.1dB of the corresponding gain, and −100dBc of the adjacent channel power rejection (ACPR) at the output power of 30dBm.

Key words: heterojunction bipolar transistor; power amplifier; bias network; gain compression; quiescent bias current
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1 Introduction

Power amplifier is a key component in mobile communication system, which directly influences the standby time and communication quality, and has been a hotspot of current research. As the mobile communication after the 3rd generation demands very low distortion and long talk time, power amplifier in mobile communication often has a strict requirement of linearity and efficiency.

In order to prolong the talk time, generally speaking, we need to improve the efficiency of the power amplifier and reduce the power dissipation. However, this can drive the transistor near the region of saturation, thus leading to gain compression and phase expansion, that is, poor linearity.

Because of nonlinear factors of the transistor, the output power deviates from the linear amplification and exhibits gain compression when the input power is above certain level, which greatly adds difficulty into linear power amplifier design[8]. Too often, designers adopt some linearized techniques, such as feedforward[4,5], cartesian[6], LINC and so on, to realize linear amplification in a wide range. On the other hand, these techniques often come along with the shortcomings of increasing the complexity and the cost, reducing the bandwidth and so on, with the result of limited applications.

In this work, we adopt and optimize a novel bias network, based on which we realize a three-stage medium power amplifier. This power amplifier consumes a quite low quiescent bias current, with each stage of 12.1, 42.2, and 55.4mA respectively, which is apparently below that of the similar product international[9]. And at the shutdown mode, the amplifier has an extremely low leakage

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current of 36.6pA. Under the operation of 3.5V, this amplifier achieved the gain up to 29.1dB, maximum linear output power of 30dBm, and a good power added efficiency(PAE) of 43.4% with the adjacent channel power rejection(ACPR) of −100dBc at IS95 Reverse Link CDMA Signal Source (1.2288MHz primary channel bandwidth, 30kHz adjacent channel bandwidth, and ±885kHz frequency offset). Thus the performance of this power amplifier has reached that of the similar product international[9].

2 Device design

HBT device has such the virtues as high power density, high drive ability, low phase noise, high linearity, single voltage operation, and a relatively low requirement of lithography precision, which make it especially applicable for power amplifier. In this work, we adopt InGaP/GaAs HBT with extramely reliable.

In practical, an emitter with long length can result in thermal failure. On the other hand, when the emitter width falls below a certain value, the influence of parasitic parameters increases greatly and lowers f_{max}. In this work, we adopt the HBT with 3μm × 15μm of emitter size, which can balance both the frequency performance and the drive ability[10].

As the current density in HBT is very high during the work, the device temperature arises quickly with the influence of the self-heating and the heat dissipation from nearby devices. Positive feedback between the temperature and current can worsen device performance, or even lapse. Thus, the dissipation condition of the circuit and the thermal stability of the semiconductor material play a key role in HBT reliability.

To prevent the thermal collapse in HBT, we extracted the parameters from a cell formed by three transistors in parallel and the circuit adopts multi-cell in parallel as shown in Fig. 1. This way not only reflects the realistic performance of the devices, but also takes the thermal effect into consideration, which can make the model in highly accordance with practical work and prevent the thermal collapse in a maximum length.

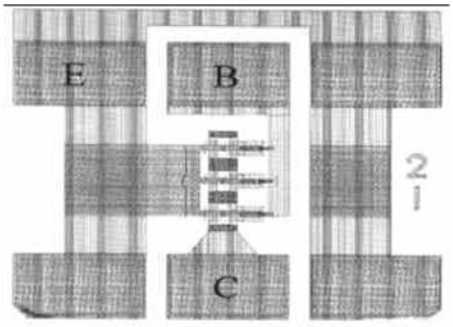

Fig. 1 HBT layout of three fingers used in parameters extraction

Too often people use the ballasting resistor in serial connection with the emitter or the base, in order to balance the current and meliorate the thermal distribution. On the other hand, the resistance can also affect the frequency performance of the transistor and the power gain of the circuit, which demands a trade-off decision.

When people adopt the way of base ballasting resistance, generally they use a capacitor in parallel connection with resistor. This kind of design not only adds the complexity into layout design, but also has a shortcoming of the ballasting effect existing only in DC condition. Thus in this work, we adopt the way of emitter ballasting resistance to increase the stability, which can realize the negative feedback not only in DC condition, but also in RF condition, and thus the thermal collapse can be prevented more effectively. According to Ref. [1], the optimal emitter resistance needed to prevent the collapse is given below

$$R_{E\text{-}opt} = R_{th11}\varphi BV_{CEO}(1-\zeta)$$

where $\zeta = 2\left[\frac{\eta kT_A}{q} \times \frac{1}{I_{max}R_{th11}\varphi BV_{CEO}}\right]^{1/2}$, φ is the thermal-electrical feedback coefficient, equal to 1.0mV/℃; η is the collector current ideality factor, equal to 1.1. Namely, both of φ and η are independent of temperature or current level; I_{max} is the maximum collector current; ζ is thermal stability factor. The HBT is thermally stable if $\zeta \geqslant 1$ and no ballasting resistance is needed.

When $\zeta < 1$, finite emitter ballasting resistance must be added to prevent the collapse. R_{th11} is thermal resistance of finger 1 due to power dissipation in finger 1. According to the relationship between the thermal resistance and substrate thickness of the HBT with 3μm × 15μm of emitter size in Fig. 2[2].

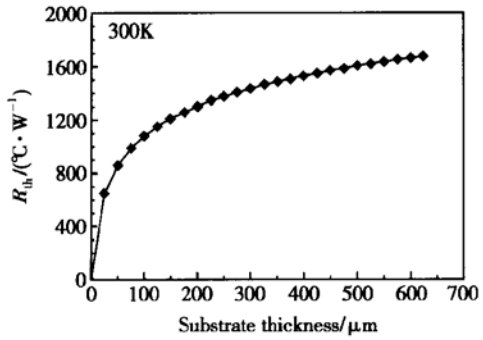

Fig. 2 Thermal resistance versus substrate thickness

Here R_{th11} is 1000 ℃/W as our substrate thickness is thinned to 100μm.

Accoreding to the equation, we can get the emitter resistance needed to keep the stability. After we subtract the emitter intrinsic resistance and the ohmic contact resistance from the resistance calculated, resistance needed in serial connection with the emitter outside is about 2.5Ω. And through simulation, we find the added resistance of 2.5Ω affects the frequency performance of the HBT slightly, so the effect on the frequency performance can be ignored in this case as shown in Fig. 3.

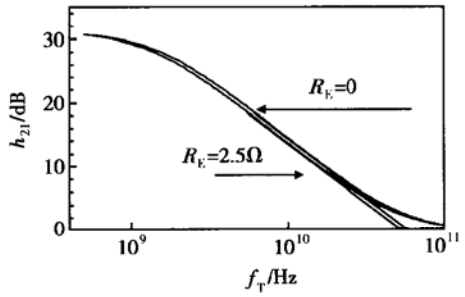

Fig. 3 Simulation result of frequency performance dependences of emitter ballasting resistance

3 Circuit design

Figure 4 shows that the power amplifier consists of a three-stage cascaded circuit. According to the power assignment, the circuit consists of a high-pass input matching network, a driver stage HBT with 3μm × 15μm × 6 of emitter size, a middle stage HBT with 3μm × 15μm × 24 of emitter size, a power stage HBT with 3μm × 15μm × 64 of emitter size, and a high-pass interstage matching network, together with an output matching network. The input stage and output stage are matched to the characteristic impedance of 50Ω, with the input VSWR of only 1.7. On the other hand, to achieve passive components with high Q, we leave the output matching network and part of bias networks outside of the die, which can not only make up for the problem brought by the process tolerance variation, but reduce the cost.

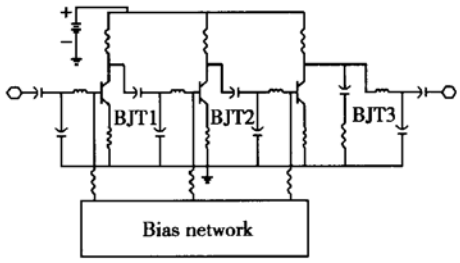

Fig. 4 Circuit schematic of the ISM three-stage power amplifier

In order to achieve high efficiency and high linearity simultaneously, we bias the 1st stage near the class A operation while the rest of the stages are biased near class B. Thus the quiescent bias current of the three stages is separately 12.1, 42.2, and 55.4mA, which is obviously below that of the similar kind of product international[9]. And at the shutdown mode, the power amplifier has an extremely low leakage current of 36.6pA. Obviously, both of them are favorable for the lower power dissipation and the longer work time, making the power amplifier more applicable for the mobile applications.

4 Design of bias network

Here we adopt the bias network[3] shown in Fig. 5. This kind of bias network not only can realize the compensation for the temperature variation with the use of diodes, but also help to increase the drive ability of the amplifier, and improve the linearity through the discharge of C17.

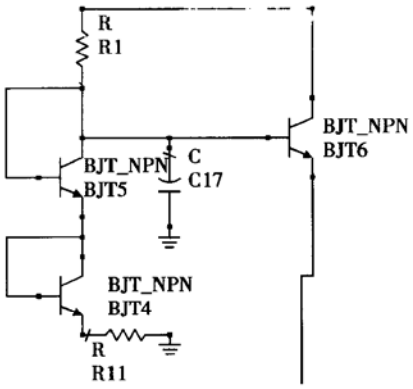

Fig. 5 Traditional bias circuit

It is known to all, the nonlinear characteristics of the transistors make the amplifier deviate from the linear amplification and exhibit gain compression when the input power reaches certain value. When the gain compression reaches 1dB, the corresponding output power is so called P_{1dB}. Though the bias network adopted can improve the linearity effectively, in practical design we find that, with the quiescent bias current being reduced, the class AB power amplifier also appears gain compression even at the low input power level. As shown in Fig. 6, there appears signal distortion at small signal operation. Also in Fig. 7, the amplifier does not amplify linearly at a constant gain, even at the small signal operation, which is, obviously, not what we expect and will definitely affect applications.

On one hand, there is a base-emitter capacitance of C_{je} at BJT6 (Fig. 5). If we ignore the diffusion capacitance, the capacitance at the BE junction is determined by the depletion capacitance and can be expressed as[1],

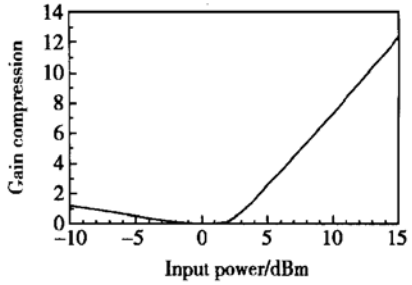

Fig. 6 Simulation result of gain compression versus input power

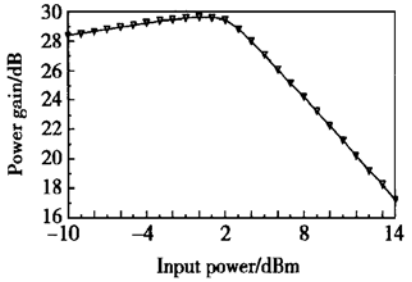

Fig. 7 Simulation result of power gain versus input power

$$C_{je} = \frac{\varepsilon_0 \varepsilon_r A_{be}}{W_{de}}$$

$$W_{de} = \sqrt{\frac{2\varepsilon_0 \varepsilon_r (\Phi_{be} - V_{be})}{qN_{ne}}}$$

$$\Phi_{be} = E_{ge} - \Delta E_v$$

$$A_{be} = N_e (W_e - 2S_{ecut})(L_e - 2S_{ecut})$$

where ε_r is the relative dielectric constant of InGaP, and here it equels 11.9; A_{be} is the area of emitter junction, and S_{ecut} is the undercut of the emitter; N_e is the factor of emitter; Φ_{be} is BE junction built-in potential, which is dependent on E_{ge} of InGaP and the ΔE_v of the heterojunction of InGaP/GaAs. Here E_{ge} equels 1.85eV, and ΔE_v equels 0.33eV; N_{ne} is doping concentration in InGaP layer, which is $3 \times 10^{17} cm^{-3}$ according to our epitaxy wafer. Thus the BE junction capacitance is about 117 fF in the HBT with the emitter sizes of 3μm × 15μm.

According to our analysis, the problem mainly lies in the current distraction effect. The BE junction capacitance of BJT6 is in a serial connection with C17. After that, the capacitance after the serial connection connects in parallel

with the BE junction capacitance of BJT(1, 2, 3) (Fig. 4). Thus this results that the input signal will be distracted to the branch of the bias network, that is, the path of the serial connection of BJT6 and C17, which makes the input power relatively low and gain decreased.

In order to solve this problem, we optimize the network design by adding an additional inductor, L18, shown in Fig. 8. Because of the inductance, signal distraction is prevented at small signal operation. When the input signal is large, besides preventing the signal distraction, the self-inductance can partly prevent over discharge of C17. Thus the optimization can realize linear amplification in a wider range.

Take the last stage as example, BJT6 is composed of six HBTs in parallel connection, and thus the BE junction capacitance is 702fF (6 × 117fF). If the capacitance of C17 is 5pF now, the capacitance after the serial connection(Fig. 5) is 616fF, equals to 108Ω($1/\omega C$). While BE junction capacitance of BJT3 in the main path of the circuit is 7.5pF, the capacitive reactance is 9Ω. Thus there will be 8 percent of the current distracted. If the inductance of L18 that we add is 5nH, the capacitive reactance is 75Ω(ωL). And now there will be only 5 percent of current distracted. According to the equation of $P \propto I^2$, the distraction effect after optimization can reduce the power loss by 61% compared to that in the before.

As far as the 2nd stage, BJT6 is composed of four HBTs, and the BE junction capacitance is 468fF. If the capacitance of C17 is 5pF, the capacitance after the serial connection(Fig. 5) is 428fF, which is equal to 155Ω. While the BE junction capacitance of BJT2 in the main path of the circuit is 2.8pF, the capacitive reactance is 24Ω. Thus 13.4 percent of the current will be distracted. If the inductance of L18 is 5nH now, then the capactive reactance is 75Ω. Now only 9 percent of current will be distracted. As is seen from above, the distraction effect after optimization is reduced by 55% compared to that in the before. Therefore, the influence of the distraction after optimization is reduced greatly.

At large signal operation, according to $g_e = \frac{qI_E}{\eta kT}$, the internal resistance of BJT(1, 2, 3) decreases with the increase of the current, the effect of distraction is relatively low compared to that at the small signal operation. At the same time, the input signal is sin signal while discharge of C17 works by the exponent law. The difference can be compensated by the self-inductance through preventing over discharge of C17. Therefore, the power amplifier after optimization exhibits quite low gain compression at a relative wider range of signal operation. And it is not until the input power is quite large that the amplifier begins to appear the normal gain compression.

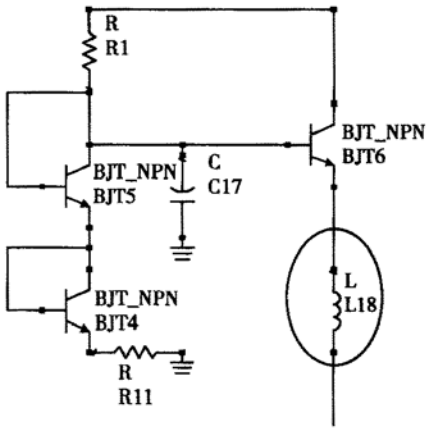

Fig. 8 Bias circuit after optimization

Comparing Fig. 10 with Fig. 6, we can find that the small signal gain compression of 1.2 at input power of −10dBm in Fig. 6 is almost eliminated in the result in Fig. 10 after optimization. Through the comparison of Figs. 11 and 7, we also can find that, the power gain, which is less than 28dB at the input power of −10dBm, rises to 29.1dB after optimization, which is the same as the gain at the input signal of 0dBm. The results above show that the design after optimization can realize linear amplifica-

tion in a wide range and can effectively solve the problem of gain compression at the small signal operation.

5 Performance analysis

As we adopt some novel techniques in the work, the final performance is satisfing. Under the operation of 3.5V, the three-stage power amplifier consumes very low quiescent bias current, separately 12.1, 42.2, and 55.4mA. This amplifier achieves the gain up to 29.1dB (Figs. 9 and 13), maximum linear output power of 30dBm (Figs. 12 and 11) and a good power added efficiency (PAE) of 43.4% at the output power of 30dBm (Fig. 10), when an adjacent channel power rejection (ACPR) can reach −100dBc(Fig. 14). From the results, we can see that the power amplifier in this work owes the virtues of high power gain and high power added efficiency and linearity, which reach the performance of the similar product international[9].

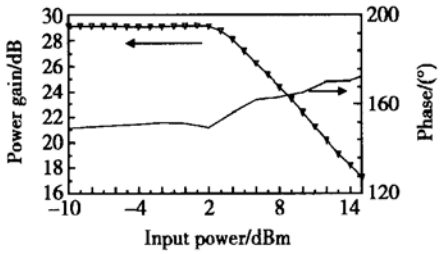

Fig. 9 Simulation results of power gain and phase deviation versus input power after optimization

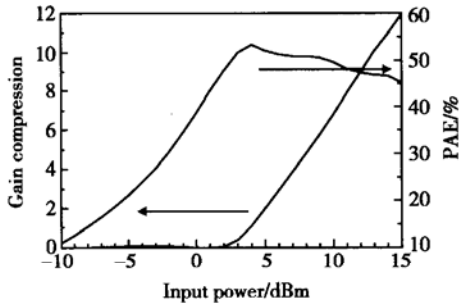

Fig. 10 Simulation results of gain compression and PAE versus input power after optimization

6 Conclusion

Through the optimized bias network, a three-stage medium power amplifier at ISM band is realized based on the large-signal model extracted from InGaP/GaAs HBT. This power amplifier consumes very low quiescent bias current, with each stage of 12.1, 42.2, and 55.4mA re-

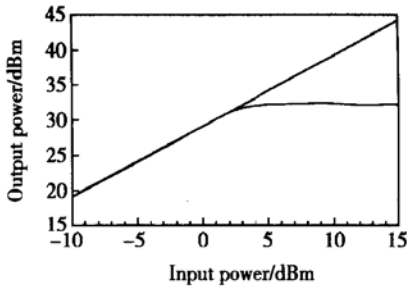

Fig. 11 Simulation result of output power versus input power after optimization

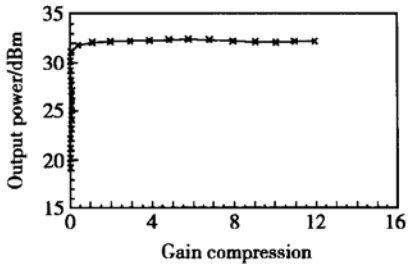

Fig. 12 Simulation result of output power versus gain compression after optimization

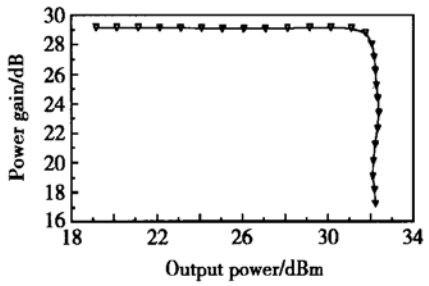

Fig. 13 Simulation result of power gain versus output power after optimization

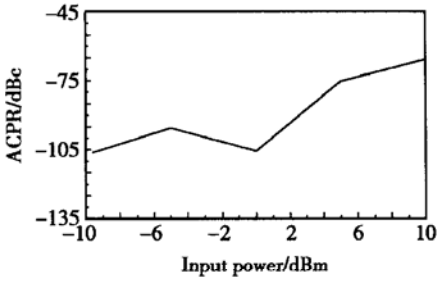

Fig. 14 Simulation result of ACPR versus input power after optimization

spectively, which is obviously below that of the similar product international. At the mode of shutdown, the amplifier consumes an extremely low leakage current of 36.6pA. This amplifier achieves the gain up to 29.1dB, maximum linear output power of 30dBm, when the good power added efficiency of 43.4% and the adjacent channel leakage power ratio can reach - 100dBc at IS95 Reverse Link CDMA Signal Source (1.2288MHz primary channel bandwidth, 30kHz adjacent channel bandwidth, and ±885kHz frequency offset). Therefore, the power amplifier in this work is especially favorable for the mobile applications.

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ISM 频段中功率功率放大器*

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摘要: 采用三指单胞的 InGaP/GaAs HBT 提取的大信号模型参数, 设计出应用于 ISM 频段的三级 AB 类功率放大器. 通过对传统偏置网络的优化, 消除了小信号下的增益压缩. 在 3.5V 电压下, 该放大器的最大线性输出功率为 30dBm, 增益达到 29.1dB, 对应的功率附加效率为 43.4%, 临近沟道抑制比达到 - 100dBc, 而静态偏置电流很低, 只有 109.7mA.

关键词: 异质结双极型晶体管; 功率放大器; 偏置网络; 增益压缩; 静态偏置电流

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