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Design and Test of a CMOS Low Noise Amplifier in Bluetooth Transceiver*

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Abstract: A RF low noise amplifier, integrated in a single bluetooth transceiver chip and fabricated in 0.35μm digital CMOS technology, is presented. Under the consideration of ESD protection and package, design methodology is discussed from the aspects of noise optimization, impedance match, and forward gain. At 2.05GHz, the measured S_{11} is −6.4dB, S_{21} is 11dB with 3dB-BW of 300MHz, and NF is about 5.3dB. It indicates that comprehensive consideration of parasitics, package model, and reasonable process is necessary for RF circuit design.

Key words: CMOS low noise amplifier; noise figure; impedance match; bluetooth transceiver
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1 Introduction

Wireless communication triggers the research and development of RF integrated circuits (RF IC), and the rapid growing market for more portable and cost equipments motivates the single chip with RF front-end and digital processor integrated together. This trend makes CMOS RF IC more attractive in the competition with its counterparts.

CMOS low noise amplifier (LNA) is the backbone of RF communication receivers. Its noise performance determines the sensitivity of the whole receiver. Its gain not only affects the linearity of the next circuit block, but also defines the overall noise performance. And its impedance matching is very important for maximum power transfer. Recently, several CMOS LNAs have been reported[1,2], in which the ESD protection and package effect have not been considered. However, for commercial application, both ESD and package must be taken into account for handling and reliability reason even at the cost of degradation of the overall performance of LNA.

2 Circuit design

2.1 Noise optimization

In noise figure prediction, accurate modeling of a MOSFET is crucial and difficult. In this paper, noise optimization is performed based on the conception of correlation matrix proposed by Hillbrand and Russer[3].

The chain representation[3] of the correlation matrix

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can be obtained as[4]

$$\boldsymbol{C}_{\mathrm{A}} = 2kT \begin{bmatrix} R_{\mathrm{n}} & \dfrac{F_{\min}-1}{2} - R_{\mathrm{n}} Y_{\mathrm{opt}}^{*} \\ \dfrac{F_{\min}-1}{2} - R_{\mathrm{n}} Y_{\mathrm{opt}} & R_{\mathrm{n}} \mid Y_{\mathrm{opt}} \mid^{2} \end{bmatrix} \tag{1}$$

where R_{n}, $F_{\min}$, $Y_{\mathrm{opt}}(= G_{\mathrm{opt}} + \mathrm{j}B_{\mathrm{opt}})$ are four noise parameters, which can completely characterize the noise performance of a two-port network. $F_{\min}$ is the minimum noise factor that the network can achieve with the optimum source admittance condition ($Y_{\mathrm{s}} = Y_{\mathrm{opt}}$), Y_{s} is the source admittance, R_{n} is the equivalent noise resistance and can amplify the difference between Y_{s} and Y_{opt}.

In this paper, drain current noise i_{d} and induced-gate noise i_{g}, which one necessary for the determination of the chain representation of the correlation matrix $\boldsymbol{C}_{\mathrm{A}}$, are formulated based on the theory of channel length modulation (CLM). The corresponding equivalent circuit of an intrinsic RF MOSFET is shown in Fig. 1, where R_{i} is a channel-induced resistance considered at high frequency[5]. By this way, $F_{\min}$ and R_{n} of a MOSFET with different gate width and under different gate bias can be shown graphically in Fig. 2. It should be specified that the MOSFET under the study is in the state of saturation.

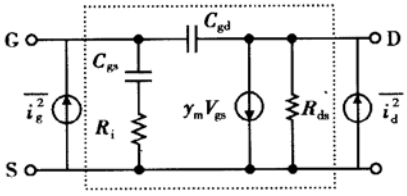


Fig. 1 Intrinsic part of a RF MOSFET

Since the gate length of a RF MOSFET is just the smallest dimension allowed by the process technology, what is needed and determined are the gate width of a MOSFET and its bias from the aspect of circuit design. In conjunction with the constraint of power consumption, in this work, the gate bias of the amplifying transistor is around 860mV, the gate width is 360μm, and the static working current is about 6.5mA.

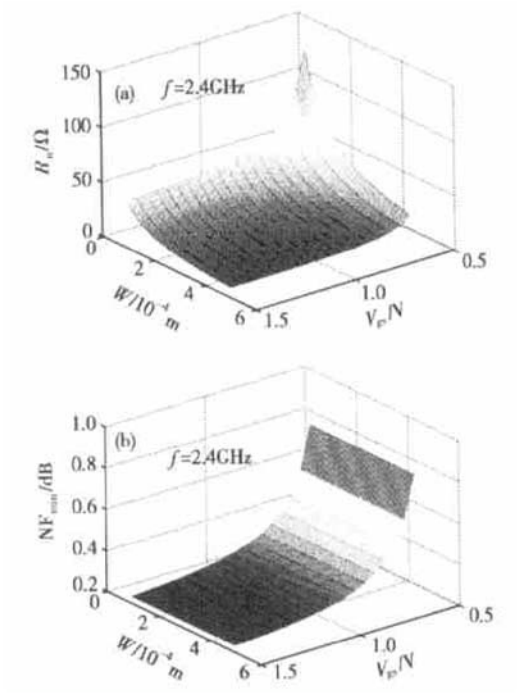


Fig. 2 R_{n} and $\mathrm{NF}_{\min}$ under different gate width and gate bias

2.2 Impedance match and forward gain

Because both of the package and the ESD protection are considered in this circuit design, impedance match is not as simple as that introduced by Lee[6]. In this case, the input stage of a LNA is shown in Fig. 3(a) with parasitic capacitances and inductances included, and C_{x} is the parasitic capacitance related to the bottom plate of the DC block capacitor.

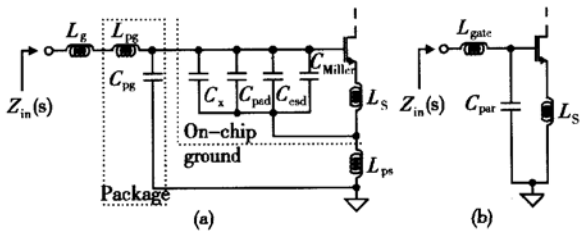


Fig. 3 Input stage with package and ESD

In order to reduce the parasitic inductance between on-chip ground and the real ground L_{ps}, the chip in this paper is connected to five parallel bondpads. Then, the input circuit can be simplified approximately as that shown

in Fig. 3(b), where

$$\begin{aligned} L_{\text{gate}} &= L_{\text{g}} + L_{\text{pg}} \\ C_{\text{par}} &= C_{\text{Miller}} + C_{\text{esd}} + C_{\text{pad}} + C_{\text{x}} + C_{\text{pg}} \end{aligned} \tag{2}$$

After a series of parallel-series transformations shown in Fig. 4, the input impedance of LNA with pad and ESD protection at resonance is

$$R' \approx \frac{R}{(1 + C_{\text{par}}/C_{\text{eq}})^2} = \frac{\omega_{\text{T}} L_{\text{S}}}{(1 + C_{\text{par}}/C_{\text{eq}})^2} \tag{3}$$

where C_{eq} is the equivalent capacitance of C_{gs} and L_{s}, ω_{T} is the cutoff frequency of the transistor. It is obvious that the existence of C_{par} requires larger L_{s} for input impedance matching, which inevitably enlarges the chip area and degrades the forward gain of a LNA. To reduce the harmful parasitic effect, some solutions have been adopted in this work: (1) the two lower-layer metals of the common pad are removed; (2) metal 4 and metal 3 are used to construct an interdigital DC block capacitor for small C_{x}; (3) the size of the cascade transistor is chosen as the same as that of the amplifying one to suppress the Miller effect.

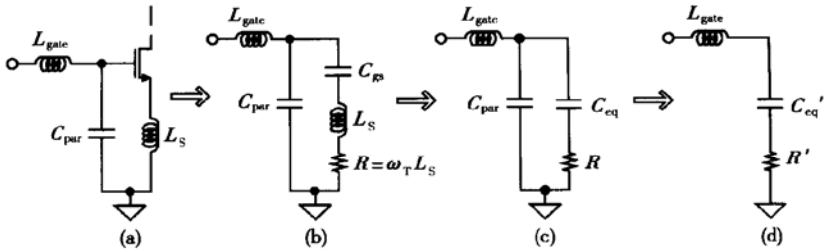


Fig. 4　Parallel-series transformation for parasitcs analysis

The provided parasitic capacitance of cascade point (merging point of M1's drain and M2's source) is small enough to draw little current separately, the current flowing through load i_2 can be assumed equal to i_1 that flows through M1, illustrated in Fig. 5. Then, the voltage gain can be expressed approximately by

$$|A_{\text{V}}| \approx \frac{\omega_{\text{T}} Q_{\text{L}} L_{\text{d}}}{R_{\text{S}} + \omega_{\text{T}} L_{\text{S}}} \tag{4}$$

where Q_{L} is the quality factor of inductor L_{d}. So for high voltage gain, the used inductor L_{d} must have large inductance and high quality factor. At the same time, the value of L_{s} is inversely proportional to the gain, which leads to a conflict between input match and high gain, especially when package and ESD protection are considered. After a trade-off, in this work, L_{s} is set to a value of 1nH, and the inductance of L_{d} is 5.6nH.

3　Circuit implementation

The circuit configuration of the LNA is shown in Fig. 6, which does not include bias circuit. It is a single-ended cascade architecture. A large capacitance C_0 is added to ensure the source of M3, a virtual ground for RF signal. The drain of M2 is the output point and connected with the input stage of the mixer, so it is not a right point for test. For this reason, an open-drain MOSFET M10 is added with the test instrument as its load. The dimension of M10 is relatively small and limited by the output frequency. The side effect of this test strategy is that the

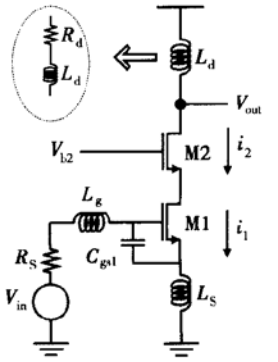


Fig. 5　Basic circuit of LNA

measured S_{21} and NF must be corrected as discussed in the next section. Note that at the right side of the broken line, it is a negative feedback circuit introduced for the purpose of stabilizing the static work condition of LNA. The simulation and measurement results are listed in Table 1.

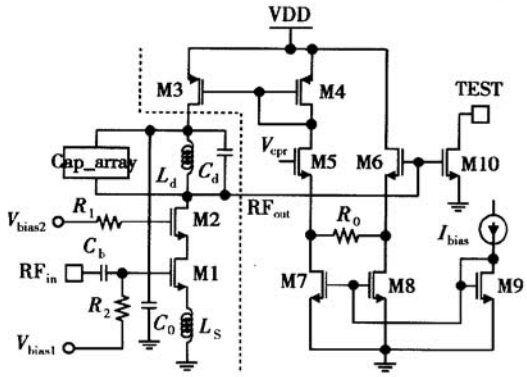


Fig. 6 Circuit diagram of LNA

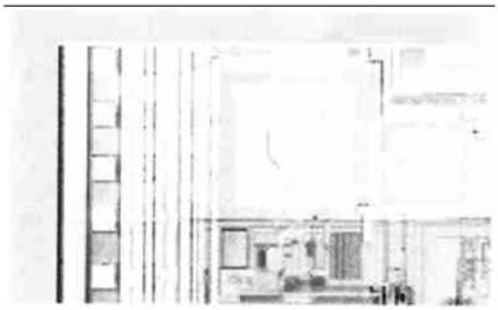


Fig. 7 Die micrograph of LNA

Table 1 Simulation and measurement results summary

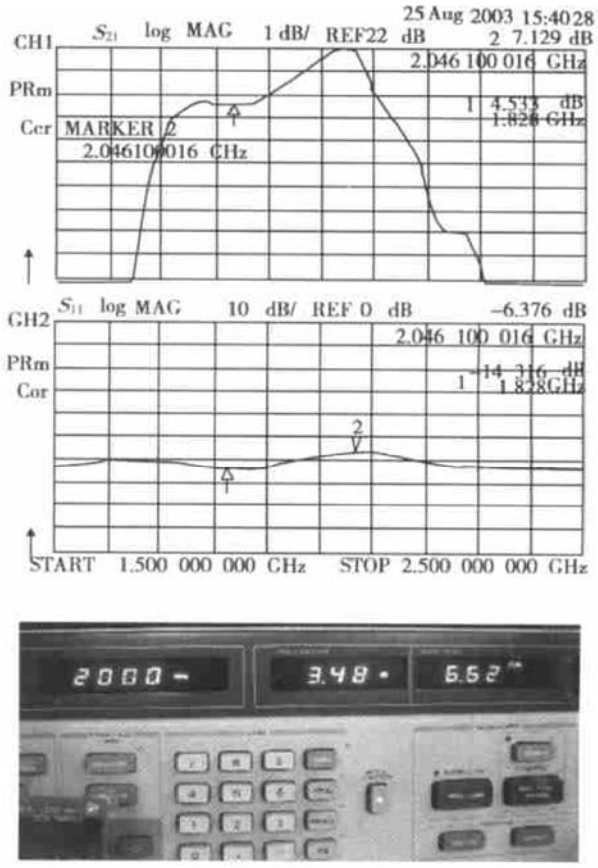
Result	Frequency /GHz	3dB-BW /MHz	NF /dB	S_{21} /dB	S_{11} /dB	I_{main} /mA	I_{test} /mA
Simulation	2.4	300	3.5	14	-8.6	7	6
Measurement	2.05	300	5.3	11	-6.4	8	5

I_{main} means the working current when M10 is off; I_{test} is the static current flowing through test transistor M10. The power supply is 3.3V.

4 Circuit measurement and analyses

The bluetooth transceiver chip was fabricated in TSMC 0.35-μm digital CMOS technology. The die micrograph of LNA is shown in Fig. 7. The test instruments are HP 8720D network analyzer for S-parameters and Agilent 8970B noise figure meter for noise measurement.

S_{21} and NF shown in Fig. 8 are the measured values at the test point (see Fig. 6). In order to get performance parameters of the LNA only, additional gain and noise from M10 should be deducted from the measurement results.



d S_{11}, S_{21}, and NF

For a two-stage cascade system shown in Fig. 9, the total gain(dB) is

$$S_{21_{tot}} = S_{21_1} + S_{21_2} \quad (5)$$

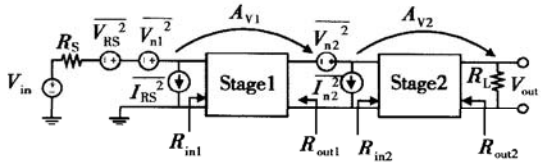


Fig. 9 A two-stage cascade system

Because the measured I_{test} is 5mA, the gate bias of M10 shifts from the designed 1.2V to 1.1V or so, at the same time, the size of M10 is 90/0.35, it is easy to obtain

the gain of the second stage S_{21_2}. The gain is 0.64 or −3.8dB for a 2GHz signal when the load is a resistance of 50Ω that is just the impedance of the test instrument. According to Eq. (5), after correction, the gain of LNA as well as S_{21_1}, is about 11dB.

Also for this cascade system, the total noise factor is expressed by[7]

$$F_{\text{tot}} = \frac{4kTR_S + \overline{(I_{n1}R_S + V_{n1})^2}}{4kTR_S} + \frac{\overline{(I_{n2}R_{out1} + V_{n2})^2}}{A_{v1}^2} \times \frac{1}{(R_{in1}/(R_S + R_{in1}))^2} \times \frac{1}{4kTR_S} \quad (6)$$

where R_s, R_{in1}, and R_{out1} are the source impedance, input and output impedance of the LNA respectively. $A_{v1} \times \frac{R_{in1}}{R_S + R_{in1}}$ is the voltage gain of LNA, expressed by A_1. Equation (6) can be rewritten as

$$F_{\text{tot}} = F_1 + \frac{F_2 - 1}{A_1^2} \times \frac{R_{out1}}{R_S} \quad (7)$$

where F_1 is the noise factor of the LNA; F_2 is the noise factor of M10 with respect to R_{out1}, and is around 1.4; R_{out1} is about 500Ω, R_s is 50Ω; F_{tot} could be derived from NF_{tot}. NF_{tot} represents the net noise figure after eliminating the noise of elements outside the chip from the measured result and its real value is 5.8dB or so. After correction, the noise factor of LNA only, F_1, is about 3.4, in other words, the noise figure of LNA, NF_1, is 5.3dB.

There is some discrepancy in the NF between the simulation and measurement. This deviation can be partly attributed to incomplete consideration of parasitics and the noise through substrate coupling, and the quite limited set of available active and passive devices[8] such as inductor and capacitor, which is the difficulty in using a digital technology for analog and RF design.

The output frequency (see Fig. 6) is determined by

$$\omega = \frac{1}{\sqrt{L_d C}} \quad (8)$$

$$C = C_d + C_{\text{array}} + C_{db2} + C_{gs6} + C_{gs10} + C_{\text{mixer}}$$

L_d of 5.6nH is selected, then the value of C is limited to 780fF by the 2.4GHz output frequency. Assumed that capacitance variation is 10%, the inductance variation is +15%, only 90fF parasitic capacitance would cause the decrease of central frequency from 2.4GHz to 2.02GHz. So the shift of central frequency is caused by the process variation and the inter-connection parasitic effect. From this aspect, analog CMOS technology is more eligible for RF circuit design. For the input resonant frequency, package parameters must be considered as well. The package parameters were not acquired until chip fabrication, the discrepancy of S_{11} between simulation and measurement highlights the indispensability of exact package model.

5 Conclusion

As an effort to meet commercial requirements, the package and the ESD protection are included in this paper. Theoretical analysis shows that parasitic effects related to ESD and package would bring additional difficulty in implementation of overall LNA performance. Based on a 0.35μm digital CMOS technology, this chip is fabricated, and some important parameters of the LNA are measured. The discrepancy between measurement and simulation demonstrates that for RF analog circuit implementation, besides comprehensive consideration and exact model of parasitics, process technology is also an important factor. Limited by its own characteristics, digital technology is not very suitable. With the help of a RF CMOS process, 0.35μm technology is fine enough to obtain a commercial single bluetooth transceiver chip with satisfying performance.

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蓝牙收发器中的 CMOS 低噪声放大器的设计与测试*

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摘要: 介绍了一种基于 0.35μm CMOS 数字工艺、集成于单片蓝牙收发器中的射频低噪声放大器. 在考虑 ESD 保护和封装的情况下, 从噪声优化、阻抗匹配及增益的角度讨论了电路的设计方法. 经测试, 在 2.05GHz 的中心频率处, S_{11}为 - 6.4dB, S_{21}为 11dB, 3dB 带宽约为 300MHz, 噪声系数为 5.3dB. 该结果表明, 射频电路设计需要全面考虑寄生效应, 需要合适的封装模型以及合理的工艺.

关键词: CMOS 低噪声放大器; 噪声系数; 阻抗匹配; 蓝牙收发器

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