

Effect of Neutral Traps on Tunneling Current and SILC in Ultrathin Oxide Layer^{*}

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Abstract: The effect of neutral trap on tunneling current in ultrathin MOSFETs is investigated by numerical analysis. The barrier variation arisen by neutral trap in oxide layer is described as a rectangular potential well in the conduction band of SiO₂. The different barrier variation of an ultrathin metal-oxide-semiconductor (MOS) structure with oxide thickness of 4nm is numerically calculated. It is shown that the effect of neutral trap on tunneling current can not be neglected. The tunneling current is increased when the neutral trap exists in the oxide layer. This simple model can be used to understand the occurring mechanism of stress induced leakage current.

Key words: tunneling current; high-field stress; ultrathin; SILC

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1 Introduction

The stress induced leakage current (SILC) is the excess low field tunneling current across a thin gate oxide after a high electric field stress. SILC, occurring before the device breakdown, has harmful influence upon the reliability of thin gate MOSFETs. Owing to the generation of the traps during the degradation, SILC can cause the degradation of data retention in the flash memory device^[1]. Various quantitative models of SILC have been proposed in literature^[2~6], differing by some features of the underlying physical mechanisms. Early models described SILC in a pragmatic way, by using a Fowler-Nordheim expression with a reduced barrier

height acting as a fitting parameter, hence insight on the physics of the process was not available. Maserjian and Zamani^[2] first proposed trap-assisted tunneling (TAT) charge-assisted tunneling, a result of positive charge generation near the Si/SiO₂ interface, accounted for the observed excess current behavior following electron injection. Olivo *et al.*^[3] proposed that the SILC resulted not from positive charge generation and accumulation within oxide, but rather from defect-related, localized weak spots near the injection interface. The trap-assisted tunneling^[4~7] resulted from the filling and empty processes of electrons via oxide neutral trap sites generated during high-field stress has been reported. Strictly speaking, however, the models remain controversial.

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In this work, we proposed a simple potential barrier model in the SiO₂ with considering the potential barrier variation caused by the new generation of neutral traps, and numerically calculated the effect of the potential barrier variation on the tunneling current.

2 Model

It is well known the neutral trap^[4-6] will be generated in oxide layer after high field stress. It is assumed that the neutral trap will cause the variation of potential barrier in SiO₂, a rectangular potential well in the conduction band of SiO₂ shown in Fig. 1. Figure 1 is a band diagram without any applied voltage across the oxide.

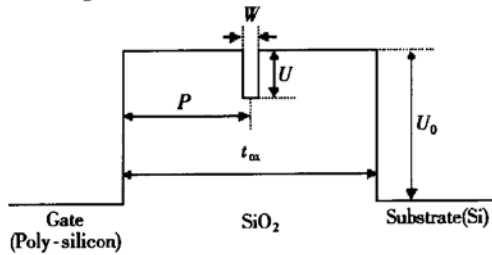


Fig. 1 Band diagram after high-field stress

In Fig. 1, U_0 is the potential barrier between Si and SiO₂; t_{ox} is the thickness of oxide layer; W , U , P are width, height, and center position of the rectangular potential well respectively induced by the neutral trap. In this article, we assume the characteristics of potential barriers variation are independent on temperature.

We calculated the transmission coefficient (TC)^[8] by solving Schrödinger equation. When the voltage V is applied to the oxide, the oxide potential barrier U_{ox} is:

$$U_{ox}(x) = U_0 - qVx/t_{ox} \quad 0 \leq x < P - W/2 \quad (1a)$$

$$U_{ox}(x) = U_0 - U - qVx/t_{ox} \quad P - W/2 \leq x < P + W/2 \quad (1b)$$

$$U_{ox}(x) = U_0 - qVx/t_{ox} \quad P + W/2 \leq x \leq t_{ox} \quad (1c)$$

A one-band effective-mass equation can be written

as:

$$-\frac{\hbar^2}{2} \nabla \frac{1}{m^*(x)} \nabla \psi + U_{ox}(x) \psi = E \psi \quad (2)$$

where m^* is the effective electron mass, \hbar is the reduced Planck's constant, and E is the electron energy.

The transmission coefficient was calculated by a numerical solution of the one-dimensional Schrödinger equation. Once $T(E, V)$ is known, the density of tunneling current is given by

$$J = \frac{qm^*}{2\pi^2 \hbar^3} \int_0^\infty T(E, V) \ln \left[\frac{1 + e^{(E_F - E)/kT}}{1 + e^{(E_F - E - qV)/kT}} \right] dE \quad (3)$$

where E_F is the Fermi energy level and q is the electron charge. So the total current is

$$I = A_0 J_0 + A_T J_T \quad (4)$$

where A_0, J_0 are areas in which there are no neutral trap and current across; A_T, J_T are areas in which there are neutral trap and current across.

3 A numerical solution of the one-dimensional Schrödinger equation

For the transmission probability across arbitrary potential barriers, instead of dealing with continuous variations of potential energy, we split up the potential barrier into segments in which potential energy can be regarded as a constant^[8,9] shown in Fig. 2. In the limit as the divisions become finer and finer, a continuous variation will be recovered.

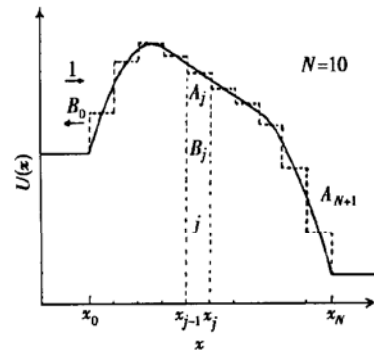


Fig. 2 Energy band diagram (solid line) and approximated potential function (dotted line) for the potential barrier

The barrier was described by N partial sub-barriers of rectangular shape which covered the whole oxide layer of thickness t_{ox} . An example, in the case where $N = 10$, is shown in Fig. 2. The potential barrier $U(x)$, the effective mass $m^*(x)$ are approximated as:

$$U(x) = U_j = [(x_{j-1} + x_j)/2] \quad (5a)$$

$$m^*(x) = m_j^* = m^* [(x_{j-1} + x_j)/2] \quad (5b)$$

for $x_{j-1} < x < x_j$ ($j = 0, 1, 2, \dots, N, N+1$)

The wave function $\psi_j(x)$ in the j th region, associated with an electron with energy E moving normally on the barrier, is given by:

$$M_l = \frac{1}{2} \begin{vmatrix} (1 + S_l) \exp[-i(k_{l+1} - k_l)x_l] & (1 - S_l) \exp[-i(k_{l+1} + k_l)x_l] \\ (1 - S_l) \exp[+i(k_{l+1} - k_l)x_l] & (1 + S_l) \exp[+i(k_{l+1} + k_l)x_l] \end{vmatrix} \quad (9)$$

and

$$S_l = m_{l+1}^* k_l / m_l^* k_{l+1} \quad (10)$$

Due to existing transmission wave only in the right of barrier, $B_{N+1} = 0$. And setting the $A_0 = 1$, we can calculate the transmission probability T as follow:

$$T(E) = \frac{m_{N+1}^*}{m_0^*} \times \frac{k_0}{k_{N+1}} \times \frac{1}{|M_{22}|^2} \quad (11)$$

In this article, if the metal-oxide interface is at the x_0 and the oxide-silicon interface at x_{N+1} , then $m_0 = m_M$ denotes an effective mass in the metal electrode and $m_{N+1} = m_{Si}$ an "effective" mass in silicon. For all other l we have $m_l = m^*$.

4 Results and discussion

Electrical transport through thin silicon oxide insulating films is mainly controlled by tunneling. This tunneling current is determined by the oxide parameters such as the interface potential barrier height and electron affinity difference between Si and SiO₂, especially for silicon oxides with thickness for less than 5nm^[11]. In this article, we considered the effect of the variation of potential barrier after the high-field stress on the tunneling current. The effects on the tunneling coefficient and the tunneling current can be obtained by using above equations. The parameters used in the calculation

$$\psi_j(x) = A_j \exp(ik_j x) + B_j \exp(-ik_j x) \quad (6)$$

where

$$k_j = \sqrt{2m_j^* (E - U_j)} / \hbar \quad (7)$$

From the continuity of $\psi_j(x)$ and $(1/m_j^*) (d\psi_j/dx)$ at each boundary, the determining A_j and B_j can be reduced to the multiplication of the following $N+1$ (2×2) matrices:

$$\begin{bmatrix} A_j \\ B_j \end{bmatrix} = \prod_{l=0}^{j-1} M_l \begin{bmatrix} A_0 \\ B_0 \end{bmatrix} \quad (8)$$

where

are $m^* = 0.5m$ (where m is the free electron mass)^[12], the oxide thickness is 4nm, and potential barrier height $U_0 = 3.15\text{eV}$ at the Si and SiO₂ interface. The width, height, and center position of potential well have different values. The potential well width (W) is less than 1nm (in the References [13, 14], the effective size of defect is considered as 1nm). The potential well height (U) is less than 2.0eV^[4, 10]. The potential well center position (P) can be arbitrary position in the oxide layer (in References [4~6], the authors thought the neutral traps' distribution is uniform.). In this paper, for the sake of simplicity, a single injecting level at the silicon conduction band edge can be assumed.

Figure 3 shows the relation between TC increments ($TC - TC_0$, TC and TC_0 are the transmission coefficient with and without the neutral trap respectively) and P at the different electric field with W being 0.3nm and U being 1.0eV. This figure shows that TC increments have the different rule when the electric field (F) across the oxide layer is different. As F is lower, the effect of potential well which is close to two interfaces including electron incidence interface and electron reflect interface will be increased. But at high electric field, the effect of potential well at the same position as above is different. The TC increments were increased at

the incidence interface. But TC increments were decreased at the reflect interface. When P is far away from the two interfaces, TC increments were increased with the increasing of the potential well's distance to the incidence interface. From this figure, we can see TC increments are increased with F increasing at the same position(P). The rules of TC increments changing with P or F are agreement due to different W and U .

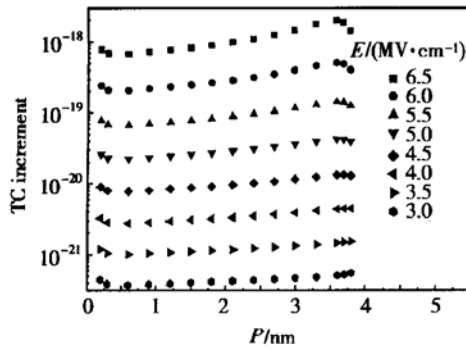


Fig. 3 Relation between TC increments and potential well position at different electric field

Figure 4 shows the relation between P and the tunneling current relative increments $(J_{gn} - J_{g0})/J_{g0}$ (J_{gn} is the tunneling current density calculated through the changed barrier caused by traps. J_0 is the tunneling current density calculated through a perfect barrier which means that there is no traps in oxide). In this article, SILC is assumed as the tunneling current density increment $(J_{gn} - J_{g0})$. It is obviously seen when the traps exist, the tunneling current is larger than that without the traps. And when the trap is at different position, the tunneling current has a different rule. When the trap is close to the incidence interface, tunneling current will be decreased with increasing P . When the trap is close to the reflect interface, tunneling current will be decreased with increasing P at high electric field and will be increased with increasing P at low electric field. When the trap is at a distance from the two interfaces, the tunneling current will be increased with increasing P . Figure 4 also shows the relation between $(J_{gn} - J_{g0})/J_{g0}$ and F . From Fig. 4, it is found the tunneling current J_{gn} is increased

with increasing E , and which agrees well with the experimental results in Ref. [5]. According to Fig. 4, $(J_{gn} - J_{g0})/J_{g0}$ and F have loose weak relativity at the incidence interface, the relativity is increased gradually from the incidence interface to the reflect interface. At the reflect interface, the relativity becomes weak again. When U and W change, the relations between $(J_{gn} - J_{g0})/J_{g0}$ and P or F have the same rules with Fig. 4. From Fig. 3 and Fig. 4, the effect of potential well which is close to the interface is different from that far away from the interface. This is interesting. Maybe we can use this to distinguish the causes of current change after high field stress, interface trap or oxide trap.

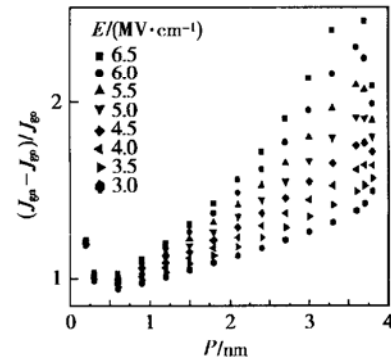


Fig. 4 Relation between $(J_{gn} - J_{g0})/J_{g0}$ and potential well center position at different electric field

In Fig. 5, the relations between TC increments or $(J_{gn} - J_{g0})/J_{g0}$ and W are given with $F = 4.5 \text{ MV/cm}$, $P = 2 \text{ nm}$, $U = 1.0 \text{ eV}$. This figure

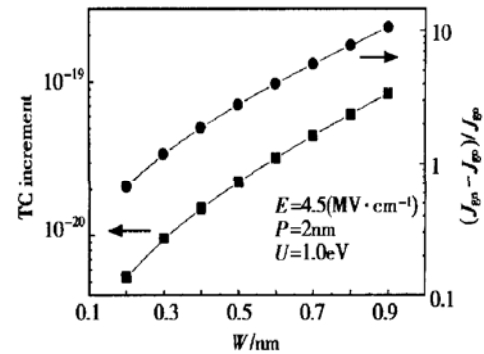


Fig. 5 Relation between TC increments or $(J_{gn} - J_{g0})/J_{g0}$ and the potential well width

shows the TC increments and $(J_{gn} - J_{g0})/J_{g0}$ are increased with increasing W . For different F , P , and U , the relations do not change. Figure 6 shows the relations between TC increments or $(J_{gn} - J_{g0})/J_{g0}$ and U with $F = 4 \text{ MV/cm}$, $P = 2 \text{ nm}$, $W = 0.2 \text{ nm}$. From this figure, we know the TC increments and $(J_{gn} - J_{g0})/J_{g0}$ are increased with increasing U . The relations do not change for different F , P , and W .

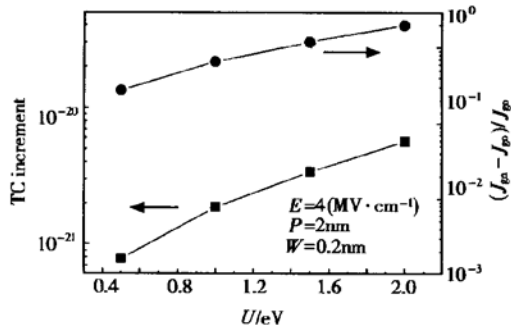


Fig. 6 Relation between TC increments or $(J_{gn} - J_{g0})/J_{g0}$ and the potential well height

From above figures, we know that the effect of potential well in oxide layer can not be neglected because it gives rise of the tunneling current increase to 10 times.

In Fig. 7, we gave the comparison of theoretical results with experimental results. In our experiments, the samples are n^+ polysilicon/ n -well nMOSFET with a gate oxide thickness of 4nm. Constant voltage gate injection stress was performed at a room temperature by using an HP4145B semiconductor parameter analyzer. The stress was periodically interrupted to perform a current-voltage (I_g - V_g) sweep. A quasi-static ramp rate was maintained during these sweeps to minimize the transient effects. Figure 7 shows the ratio of the high-field SILC (J_{SILC}) to the initial gate tunneling current density (J_{FRESH}) as a function of sweep electric field with the stress voltage 4.8V. Where $J_{SILC} = J_{Stress} - J_{Fresh}$ and J_{Stress} is gate tunneling current density after stress voltage. In theoretical calculation, for the sake of simplicity, the uniform distribution of trap, the single potential well width (0.3nm) and the single potential well height (1.0eV) were used. From Fig. 7, we know that in

this electric field range, the theoretical results agree with the experimental results well. This shows that the mechanism of SILC can be understood by this simple model.

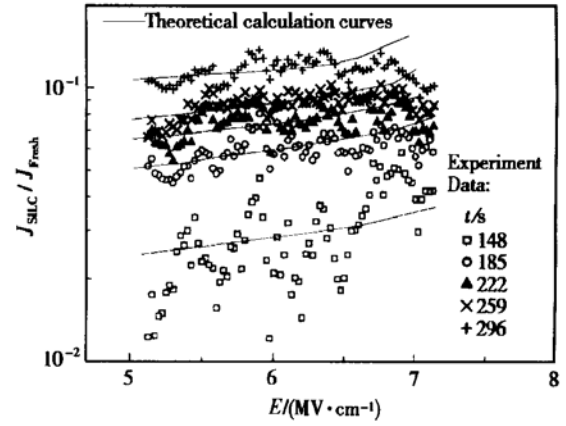


Fig. 7 Comparison between experimental data and theoretical calculation

5 Conclusion

In this paper, a simple model is given to describe the variation of the oxide layer barrier caused by the high-field stress and to show the numerical calculation of tunneling current through the oxide by solving Schrödinger equation. According to the numerical results, the effect of potential well on tunneling current in oxide layer can not be neglected. The comparison between the calculated results and the experimental data shows that this simple model can explain the mechanism of SILC qualitatively.

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超薄氧化层中的中性陷阱对隧穿电流的影响和应变诱导漏电流*

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摘要: 用数值分析的方法讨论了中性陷阱对超薄场效应晶体管(MOSFET)隧穿电流的影响. 中性陷阱引起势垒的变化在二氧化硅的导带中形成一个方形的势阱. 对于不同的势垒变化, 计算了电子隧穿氧化层厚度为 4nm 的超薄金属氧化物半导体结构的电流. 结果表明, 中性陷阱对隧穿电流的影响不能被忽略, 中性陷阱的存在使隧穿电流增加, 并且通过这个简单的模型能够理解应变诱导漏电流的产生机制.

关键词: 隧穿电流; 高场应力; 超薄; 应变诱导漏电流

PACC: 7340G; 7220H; 7340Q

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