Influence of High Temperature Treatment on the Performance of Nickel-Induced Laterally Crystallized Thin Film Transistors*

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Abstract: Well-known for their good performance, thin film transistors (TFTs) with active layers which were nickel-induced laterally crystallized, are fabricated by conventional process of dual gate CMOS. The influence of pre-high-temperature treatment of device fabrication on the performance of TFTs is also investigated. The experiment shows that the high-temperature treatment affects the performance of the devices strongly. The best performance is obtained by adopting pre-treatment of 1000℃. The mobility of $314\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$ is obtained at NMOS TFTs with pre-treatment of 1000℃, which is 10% and 22% higher than that treated at 1100℃ and without pre-high-temperature treatment, respectively. A maximum on/off current ratio of 3×10^8 is also obtained at 1000℃. Further investigation of uniformity verifies that the result is reliable.

Key words: nickel-induced lateral crystallization; thin film transistor; high-temperature treatment

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1 Introduction

Silicon-on-insulator (SOI) MOSFETs have many advantages such as high density, easy isolation, simple process as well as the possibility to be used in vertical integration. For the submicron region of the size of devices, the demand of higher integration will be more aggressive than that of any practical scale of conventional devices in the future. To achieve giga-scale integration and beyond, fabrication of devices in multiple levels would be necessary. Actually, efforts have been expended in laser recrystallization of polysilicon for stacked CMOS structures[1~4], and in selective epitaxial growth of silicon for multiple layers of SOI islands[5]. However, the application is limited by the complicated process. Thin-film-transistor (TFT) technique has been received more attention because it is a promising mean of achieving three-dimensional (3-D) integration. It has also been utilized in various 3-D circuits such as SRAM's and DRAM's[6~9]. Unfortunately, the low turn-on current, high threshold voltage, and significant variation from device to device in conventional polysilicon (ploy-Si) TFTs restrain their further applications for other 3-D structures, especially when the size of device is scaled down and supply voltage is reduced.

Metal-induced lateral crystallization (MILC) of amorphous silicon (a-Si) has been studied extensively for the application of active matrix liquid

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crystal display[10~13]. Our previous research on the Ni-MILC TFTs has found that the TFTs formed on MILC polysilicon with conventional CMOS process can improve the performance of TFT dramatically since the CMOS process is similar to a subsequent high-temperature treatment[14~16]. It is obvious that the subsequent high-temperature annealing is quite important for the performance of the TFT. In this paper, the influence of pre-high-temperature treatment of MILC TFTs fabrication processed in conventional CMOS on the performance of the TFTs are investigated. It is known that the pre-high-temperature treatment can improve the performance of TFTs effectively.

2 Experiment

Starting with silicon wafers on which 400nm-thick oxide layer had been grown, 100nm of a-Si film was deposited on the oxide by low-pressure chemical vapor deposition (LPCVD) at 550℃. After 300nm of LTO was deposited at 425℃, windows were then patterned and 7nm of Ni was deposited onto the a-Si by using an electron beam evaporator at pressure of 10^{-5}~ 10^{-6}Pa. Prior to the evaporation, the native oxide on the a-Si film was removed by dipping into dilute HF. The lateral crystallization of a-Si film was then performed in N_2(purity over 99.99%) at 560℃ for 20h in a conventional horizontal furnace. The length of MILC was found to be about 86μm, which indicates that the MILC rate is about 4.3μm/h at this temperature. The remaining Ni on the oxide was removed in H_2SO_4 : H_2O_2(4 : 1) at 70℃ after the annealing. In order to investigate the influence of subsequent heat treatment on the performance of the TFTs, the wafers were grouped into three. Groups A and B were annealed in N_2 at 1100℃ and at 1000℃ for 2h, respectively. Finally, the Group C together with Groups A and B were used as starting material for fabricating the TFT on it. Standard process of dual gate SOI CMOS was adopted to fabricate TFTs on wafers of Group A, Group B and Group C. The maximum temperature in all process was 1000℃, and the channel dose in NMOS was 4 $\times 10^{12}cm^{-2}$ with Boron. The gate oxide was thermally grown and 10nm of the oxide was obtained. In this paper, NMOS TFTs with W/L of 15/5μm were reported.

3 Results and discussions

The TEM pictures of MILC poly-Si with and without subsequent high-temperature annealing are shown in Fig. 1. Grain size of silicon larger than 1μm was observed after MILC. This shows that the MILC film has better performance than the directly deposited polysilicon. Since some defects and grain

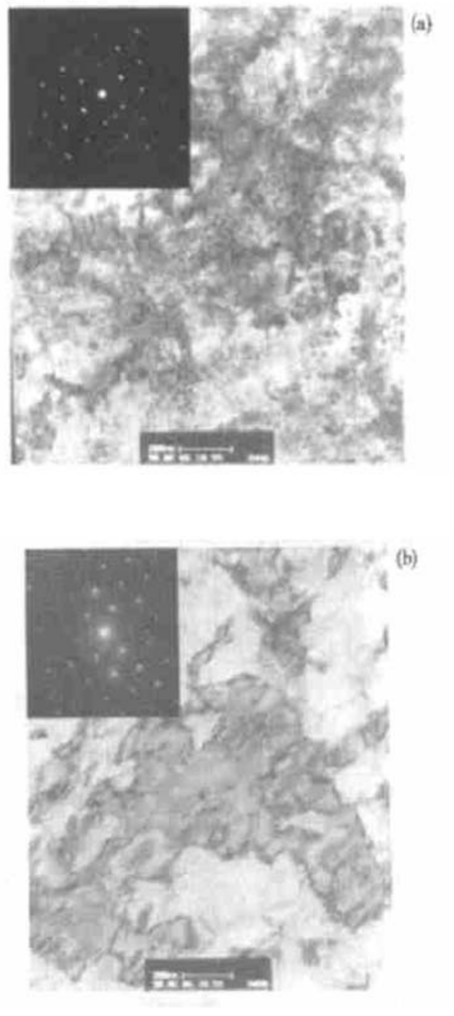

Fig. 1 TEM pictures of polysilicon film (a) Formed by Ni-MILC at 560℃ for 20h; (b) Subsequent high-temperature treatment of 1000℃ for 2h

boundary were observed from the MILC samples annealed with pre-high-temperature (Fig. 1(a)), it means that the quality of the film needs to be improved. The inset transmission electron diffraction (TED) pattern in Fig. 1(a) also reveals that the crystals formed by MILC are mainly (110) orientations. So it is possible to enhance the grain size from small grains to larger grains during high-temperature treatment. Figure 1(b) shows the TEM results after subsequent high-temperature annealing. The grain size and boundaries are clearly shown from the figure. This means that the defects are decreased and many smaller grains have been merged by subsequent high-temperature annealing. A much clear TED pattern with (110) orientation is also given in this figure.

Figure 2 shows the drain current-gate voltage (I_d-V_g) characteristics of fabricated TFTs on wafers of Group A, Group B and Group C, respectively. TFT fabricated on conventional LPCVD polysilicon film[16] is also drawn for comparison. All the devices were fabricated by standard CMOS

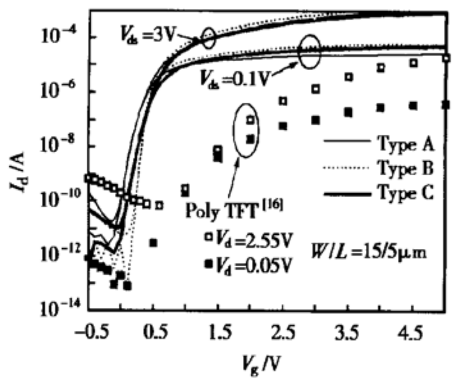

Fig. 2 I_d-V_g characteristics of the fabricated MILC NMOS TFTs with pre-high-temperature treatment of 1100℃ (Group A), 1000℃ (Group B) and without pre-high-temperature treatment (Group C)

process and the maximum temperature for the process is 1000℃. From Fig. 2, it can be found that the performance of TFTs fabricated on MILC polysilicon is much better than that of TFT fabricated on LPCVD polysilicon. That means MILC can improve the quality of the film significantly. Compared with TFTs fabricated on Groups A and C, the device fabricated on Group B has the sharpest subthreshold slope, the highest on/off current ratio of 3×10^8, a filed effect mobility of $314cm^2/(V\cdot s)$, and a threshold voltage of 0.46V. The field effect mobility was obtained from the transconductance in the linear region at V_d= 3V. The result reveals that the pre-high-temperature treatment can improve the quality of the film in both grain enlargement and decreasing or eliminating defects. It is also found that the performance of the TFT formed on Group A is slightly better than that on Group C. It means that the temperature of pre-treatment is much important for the fabrication of TFTs with good quality, and it also needs to be optimized. The reason that pre-treatment at 1100℃ is not as good as that at 1000℃ is not clearly known. But we believe that the reason is related to the secondary crystallization of MILC silicon.

The results from Fig. 2 exhibit that the pre-high-temperature treatment of 1000℃ has a large improvement on the performance of the devices compared to non pre-high-temperature treatment. A possible reason is that the secondary lateral grain growth of the MILC film is affected by the pre-existed patterns on the film. Optimized patterns can induce large elongated grains[17], but the non-optimized patterns will limit the lateral grain growth in most situations. Thus pre-high-temperature treatment can improve the quality of the film since the film is free of patterns on it. For samples of Group C, the secondary grain growth was restricted by non-optimized patterns formed at device fabrication.

Observing I_d-V_d curves of the TFTs formed on wafers of Group A, Group B, and Group C, we can not find the current induced by parasitic source/drain resistance at low V_d. This means that the ion doped MILC poly-Si layers act as a good ohmic contact material.

The performance of TFTs on different heat treatment is listed in Table 1 in detail. A reported

MILC TFT fabricated at low temperature is also listed for comparison[12]. Since the conventional process of dual gate CMOS is utilized in this work, the devices exhibit much better performance than that of reported low-temperature TFTs. Two possible reasons may explain the phenomenon. One is that the grain size of the film has been enlarged through high-temperature treatment and the defects are decreased, as shown in Fig. 1. Another may be that the doped ions at source and drain region have been activated completely compared with the situation at low temperature process[12].

Table 1 Performance of TFTs fabricated on MILC polysilicon films with pre-high-temperature treatment of 1100℃ (Group A), 1000℃ (Group B) and without pre-high-temperature treatment (Group C) A reported low temperature TFT is also listed for comparison.

	$\mu_{FE}/(cm^2 \cdot V^{-1} \cdot s^{-1})$	V_T/V	$S/(mV \cdot dec^{-1})$	I_{on}/I_{off}@ V_{DS}= 0.1V
Type A W/L= 15/5μm	282	0.53	76	1×10^8
Type B W/L= 15/5μm	314	0.46	63	3×10^8
Type C W/L= 15/5μm	258	0.56	81	8×10^7
Reported TFT with 500℃ treatment[12] W/L= 15/5μm	80	5.1	2100	3.5×10^5

The performance uniformity of the TFTs formed on poly-Si is quite important for 3-D and AMLCD applications. As the average grain size increases, variations in the number of grain boundary in the active channel region increase correspondingly and the uniformity of the devices worses progressively[16]. Unlike normally deposited poly-Si, poly-Si formed by MILC shows longitudinal elongated grains growth with primarily (110) orientated, as shown in Fig. 3. It means both performance and uniformity of the devices can be improved if the channel length is parallel to the direction of the grain growth. Our previous work has shown that the TFTs exhibit much better uniformity than conventional TFTs[16]. Figure 4 shows the uniformity of the drain current of the devices with different pre-high-temperature treatment. It is found that the uniformity of the devices with different pre-high-temperature treatments is similar to each other. This means the pre-high-temperature treatment can not significantly change the grain distribution

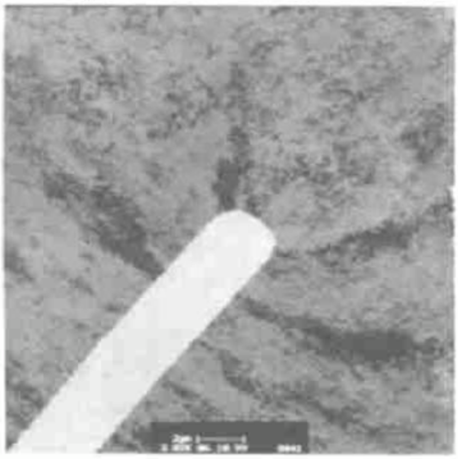

Fig. 3 TEM micrograph taken in the crystallized silicon film near the edge of nickel line The film was annealed at 560℃ for 20h.

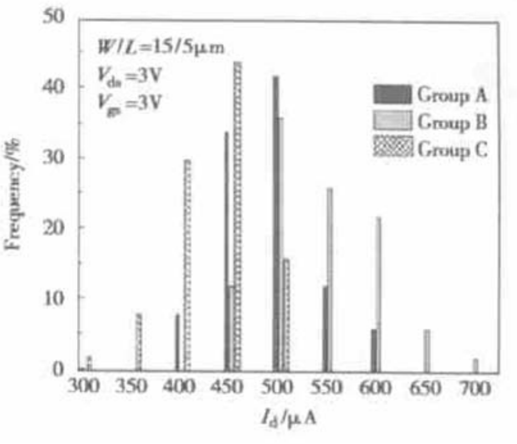

Fig. 4 Uniformity of the drain current of the devices with pre-high-temperature of 1100℃ (Group A), 1000℃ (Group B) and without pre-high-temperature treatment (Group C)

in channel regions but only improve the quality of the film. This figure also reveals that the results reported in this paper are reliable, not due to the variation in experiments and grain quality.

4 Conclusions

In summary, TFTs, which have good performance, formed on Ni-MILC polysilicon with conventional CMOS process were fabricated and characterized. TEM research indicates that the high-temperature process, including the pre-high-temperature treatment prior to the device fabrication, can enhance the grain size of silicon and decrease the defects. The fabricated TFT with pre-heat treatment of 1000℃ exhibits the mobility of $314\mu m^2/(V \cdot s)$, the threshold voltage of 0.46V, subthreshold slope of 63mV/decade, and the on/off current ratio of 3×10^8. The comparison among the TFTs with different high-temperature treatments shows that the pre-high-temperature treatment of 1000℃ can improve the performance of TFTs more obviously than 1100℃ and non pre-high-temperature treatment. This means that the pre-high-temperature treatment is quite important for the performance of fabricated MILC TFTs and the temperature of treatment also needs to be optimized.

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高温处理对镍诱导晶化硅上的薄膜晶体管性能的影响*

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摘要: 采用标准双栅 CMOS 工艺在镍诱导非晶硅横向晶化形成的多晶硅上制造了高性能的薄膜晶体管, 并详细研究了器件制备前高温预处理对薄膜晶体管性能的影响. 实验发现不同的温度处理, 将引起器件性能的显著变化. 在 1000℃预处理温度下获得了最好的器件性能. 1000℃在 NMOS 管中测得的电子迁移率达 $314cm^2/(V \cdot s)$, 分别比在 1100℃和未做高温处理下的大 10% 和 22%. 1000℃下器件的最大开关电流比也达到了 3×10^8. 对器件的进一步重复性研究证实了上述结果的可靠性.

关键词: 镍诱导横向晶化; 薄膜晶体管; 高温处理
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