A New Type of Power Clock for DSCRL Adiabatic Circuit*

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Abstract: An asymmetry power clock, 4-phase power clock supplying the power to the DSCRL(dual-swing charge recovery logic) adiabatic circuit is presented. It is much simpler than the 6-phase power clock, symmetry power clock, used in the DSCRL adiabatic circuit. Although the 4-phase power clock is simpler, the DSCRL adiabatic circuit still shows good performance and high efficiency of energy transfer and recovery. This conclusion has been proved by the result of the HSPICE simulation using the 0.6μm CMOS technology.

Key words: DSCRL adiabatic circuit; low-power; 4-phase power clock; energy recover
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1 Introduction

Reducing the power dissipation of the digital circuit systems becomes more and more important as the circuit's scale becomes larger and larger, especially in the portable and battery operated systems. Adiabatic circuits have shown a great potential for practical application in the power saving field in the future[1]. Both the adiabatic loss and the non-adiabatic loss of the circuit can be greatly reduced in the adiabatic circuits. Generally, the power clock of the adiabatic circuit is complex, which is one of the key problems in application, particularly in the full-adiabatic circuit[2]. The DSCRL adiabatic circuit is one of the best semi-adiabatic circuit which has much higher efficient energy transfer and recovery than the other semi-adiabatic circuits, such as 2N-2N2D、ADL、2N-2N2P and ECRL etc[3~7]. However, the DSCRL adiabatic circuit needs six-phase power clock to supply power, which is very complex in the semi-adiabatic circuits though it is much simpler in comparing to some power clocks of the full-adiabatic circuits.

A new power clock system, the 4-phase power clock, is proposed in the article for the DSCRL adiabatic circuit. It is an asymmetry power clock system which reduces the power clock system's complexity while the DSCRL still works for the stage of high efficient energy transfer and recovery.

2 Operation of the DSCRL

The working mechanism of the DSCRL supplying by the 4-phase power clock is introduced here. The basic DSCRL inverter circuit is given in Fig. 1. There are two main parts in the circuit, the logic operation and the load driven function. The logic operation circuit consists of two

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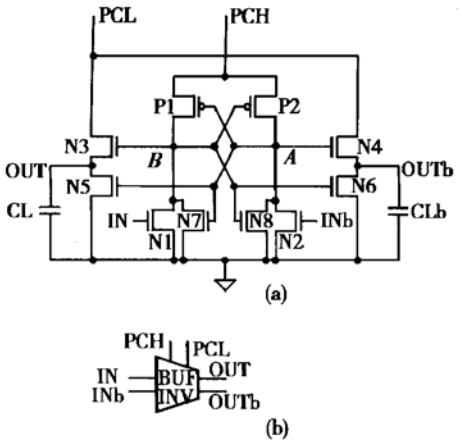

Fig. 1 (a) Schematic of the DSCRL inverter; (b) Symbol of the DSCRL inverter

PMOS transistors (P1, P2) and two NMOS transistors (N1, N2). The load driven circuits consist of the two NMOS transistors (N3, N4), which isolate the nodes B A from the load capacitance CL and CLb, separately. The power dissipation of the DSCRL is almost independent on load capacitance. The NMOS transistors (N5, N6) can ensure that circuit work well even if the load capacitance is very small. The NMOS transistors (N7, N8) ensure that the NMOS transistors (N3, N4) turn off when the voltage of the nodes B and A are 'zero', separately. A DSCRL inverter is driven by two different power clocks (PCH, PCL). V_{DH}, the amplitude of the PCH, must be greater than (V_{DL}+ V_{th}) at least, where V_{DL} is amplitude of the PCL and V_{th} is the threshold voltage of the NMOS transistor. Supposing the inverter is driven by the (PCH1, PCL1), shown in Fig. 2(a), we can divide one period of the power clocks into eight equal parts, t_1 t_2 t_3 $\cdots t_8$. Supposing IN= '0' and INb= '1', given in Fig. 3(a), then the N1 turns off and the N2 turns on. During the period [t_1, t_8], the voltage of the node A is the same as the ground while the

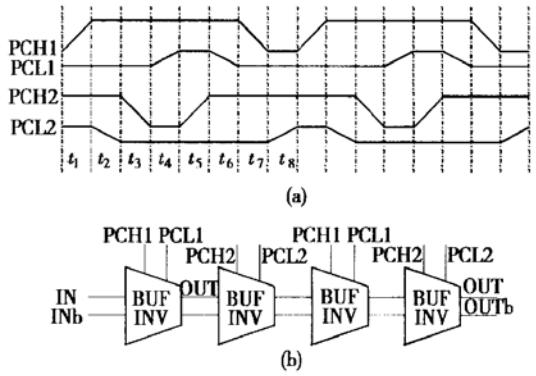

Fig. 2 (a) Four-phase power clock; (b) DSCRL inverter chain

voltage of the node B changes with the PCH1 till to $|V_{tp}|$, where V_{tp} is the threshold voltage of the PMOS transistor. During the period [t_4, t_6], the N3 turns on and the N5 turns off so the voltage of the load capacitance, CL, follows the PCL1 completely, which is a full-adiabatic process. Moreover, there is no threshold loss in the NMOS transistor N3 because the V_{DH} is bigger than (V_{DL} + V_{tn}). At the same time, the voltage of the load capacitance, CLb, is zero because the N4 turns off and N6 turns on. During the 7th period, t_7, the power clock PCKH1 begins to decrease till zero while the node B begins to discharge and its voltage begins to decrease till to $|V_{tp}|$. The informa-

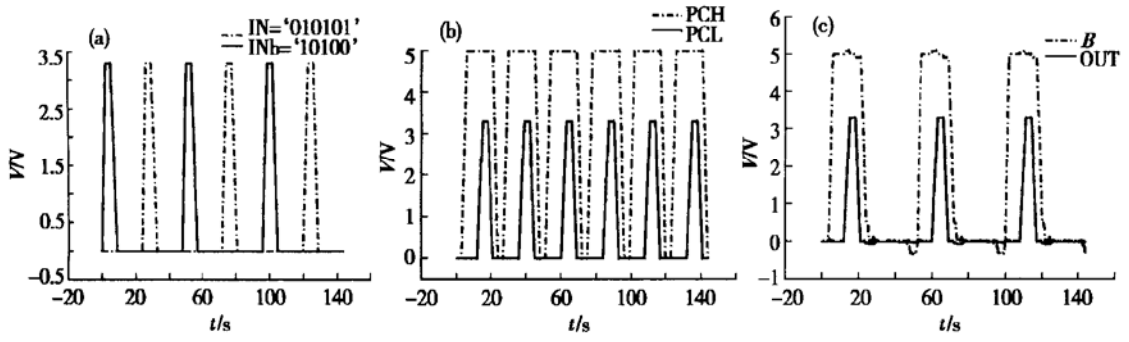

Fig. 3 (a) Waveforms of the input; (b) Waveforms of the clocks; (c) Waveforms of the nodes

tion is transferred to the next inverter (or next DSCRL circuit cell) during the 5th period, t_5. The waveforms of the B and CL are shown in Fig. 3. The new 4-phase power clock (PCH1、PCL1、PCH2、PCL2) can supply power to the DSCRL adiabatic circuit system as well as the 6-phase power clock. The operation of the DSCRL adiabatic circuit driven by the 4-phase power clocks is the same as that driven by the 6-phase power clocks. The waveforms of the 6-phase power clocks are given in Fig. 4(a). An inverter chain of the DSCRL is illustrated in Fig. 4(b).

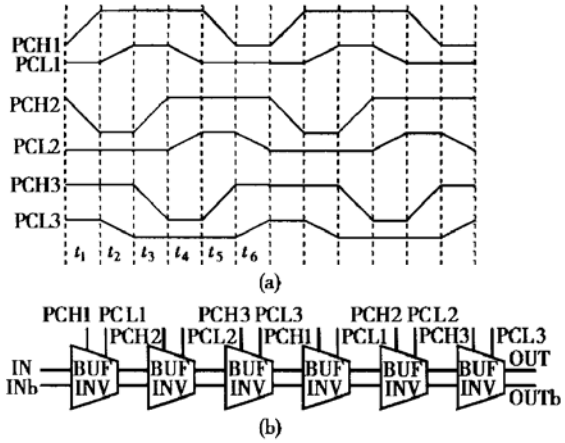

Fig. 4　(a) Six-phase power clock; (b) DSCRL inverter chain

3　Energy dissipation analysis and simulation

The energy dissipation occurs while the nodes of the DSCRL adiabatic circuit are charging or discharging, which is regarded as the main part in the total energy dissipation. The static energy dissipation caused by the leakage current is little and can be ignored. The total energy dissipation per cycle can be represented by the equation (1) as follows:

$$E_D = 2\left(\frac{R_n R_L}{T}\right) C_L V_{DL}^2 + 2\left(\frac{R_p C_{INT}}{T}\right) C_{INT} V_{DH}^2 + |V_{tp}|^2 C_{INT} \quad (1)$$

where C_L is the load capacitance, R_n is the turn-on resistance of the NMOS transistor N3(N4), T is the transition time of the power clock PCL(PCH), and V_{DL} is the amplitude of the PCL. C_{INT} is the capacitance of node A (B), R_p is the turn-on resistance of the PMOS transistor P1(P2), V_{DH} is the amplitude of the power clock PCH, and V_{tp} is the threshold voltage of the PMOS (P1 or P2). In Eq. (1), the first term represents the full-adiabatic energy consumption of the NMOS transistors (N3, N4) which are represented by E_{PCH} in Table 1. The

Table 1　Energy consumption of the dscrl inverter simulated in the different power clocks

Items / Cap	f = 4.1625MHz				f = 41.625MHz				f = 31.21875MHz	
	4-DSCRL		6-DSCRL		4-DSCRL		6-DSCRL		4-DSCRL	
C_L/pF	E_{PCH} /(pJ·cycle^{-1})	E_{PCL} /(pJ·cycle^{-1})	E_{PCH} /(pJ·cycle^{-1})	E_{PCL} /(pJ·cycle^{-1})	E_{PCH} /(pJ·cycle^{-1})	E_{PCL} /(pJ·cycle^{-1})	E_{PCH} /(pJ·cycle^{-1})	E_{PCL} /(pJ·cycle^{-1})	E_{PCH} /(pJ·cycle^{-1})	E_{PCL} /(pJ·cycle^{-1})
0.01	0.03093	0.00169	0.02718	0.00118	0.1185	0.01412	0.09724	0.01024	0.09724	0.01062
0.05	0.03089	0.00312	0.02719	0.00223	0.1186	0.02735	0.09728	0.02026	0.09728	0.02065
0.1	0.03087	0.00642	0.02714	0.0047	0.1186	0.05868	0.09725	0.04398	0.09725	0.0444
0.15	0.03086	0.01144	0.02714	0.00847	0.1185	0.1059	0.09723	0.07982	0.09723	0.08027
0.2	0.03086	0.01817	0.02713	0.01353	0.1185	0.1686	0.0972	0.1275	0.0972	0.128
0.25	0.03085	0.02661	0.02713	0.01988	0.1184	0.2464	0.09717	0.1867	0.09717	0.1872
0.3	0.03085	0.03674	0.02713	0.02751	0.1183	0.3389	0.09708	0.2573	0.09708	0.2579
0.35	0.03084	0.04857	0.02713	0.03643	0.1183	0.446	0.09704	0.3391	0.09704	0.3397
0.4	0.03084	0.06207	0.02712	0.04661	0.1182	0.5672	0.09699	0.4319	0.09699	0.4326
0.45	0.03085	0.07724	0.02712	0.05806	0.1181	0.7022	0.09694	0.5355	0.09694	0.5362
0.5	0.03084	0.09408	0.02712	0.07077	0.1179	0.8508	0.09687	0.6498	0.09688	0.6506
0.55	0.03083	0.1126	0.02712	0.08473	0.1178	1.013	0.09681	0.7746	0.09681	0.7754
0.6	0.03082	0.1327	0.02712	0.09995	0.1177	1.187	0.09674	0.9097	0.09674	0.9105
0.65	0.03082	0.1545	0.02711	0.1164	0.1175	1.375	0.09666	1.055	0.09666	1.056
0.7	0.0308	0.1779	0.02712	0.1341	0.1174	1.574	0.09657	1.21	0.09657	1.211
0.75	0.0308	0.2029	0.02711	0.1531	0.1172	1.785	0.09648	1.375	0.09648	1.376
0.8	0.03079	0.2296	0.0271	0.1733	0.117	2.007	0.09638	1.549	0.09638	1.551
0.85	0.03078	0.2579	0.0271	0.1947	0.1168	2.241	0.09627	1.733	0.09628	1.735
0.9	0.03077	0.2878	0.02709	0.2173	0.1165	2.484	0.09616	1.926	0.09616	1.928
0.95	0.03076	0.3192	0.02709	0.2412	0.1163	2.738	0.09604	2.128	0.09604	2.13

second term also represents an adiabatic energy consumption of the PMOS transistors (P1, P2). However, the third term represente a non-adiabatic energy consumption of the PMOS transistors (P1, P2) and the NMOS transistors (N1, N2). The total energy dissipation in the PMOS transistors (P1, P2) and the NMOS transistors (N1, N2) is represented by E_{PCL} in Table 1.

If the transition time T is much greater than the value of (RC), the energy dissipation of the DSCRL circuit is almost a constant, $|V_{tp}^2| C_{INT}$. The energy dissipation of the DSCRL inverter driven by the 4-phase power clock is almost the same as that driven by the 6-phase power clock. The curves of the total energy dissipation versus load capacitance are labeled E_1 and E_2 in Fig. 5. The power dissipation (E_{PCH}, E_{PCL}) of the DSCRL inverter driven by the 4-phase power clock and the 6-phase power clock are also given in Table 1. The frequency of the both

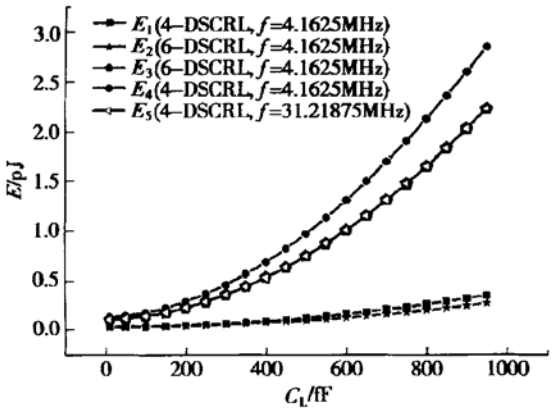

Fig. 5 Power consumption versus load capacitance

power clocks is 4.1625MHz and the transition time T of the 4-phase power clock and 6-phase power clock are 30ns and 40ns, respectively. However, if the load capacitance C_L is much greater than internal capacitance C_{INT} and the value of the (RC) is greater than transition time T, the non-adiabatic energy dissipation corresponding to the third term in Eq. (1) can be ignored. In Fig. 2(a), one period of the 4-phase power clock is divided into eight equal parts, $T = t_1 = t_2 = \cdots = t_8$, while that is divided into six equal parts, $T = t_1 = t_2 = \cdots = t_6$ in the 6-phase power clock, given in Fig. 4(a). From Eq. (1), we know that the energy consume in the DSCRL is almost the same if the transition time T in the 4-phase power clock is equal to that in the 6-phase power clock, but the frequency of the 4-phase power clock is 75% of the 6-phase power clock. The corresponding curves, labeled E_3 and E_5, overlap in Fig. 5. Table 1 also gives the corresponding energy consumption (E_{PCH}, E_{PCL}). The frequency of the 4-phase power clock is 31.21875MHz and the frequency of the 6-phase power clock is 41.625MHz. The transition times T of the both power clock are equal, $T = 4$ns. If the frequency of the 4-phase power clock is equal to that of the 6-phase power clock, then the transition time T of the 4-phase power clock is 75% of that of the 6-phase power clock. It means that power dissipation of the DSCRL in the 6-phase power clock is 75% of that in the 4-phase power clock. The corresponding curves labeled E_3 and E_4 are illustrated in Fig. 5. The frequency of the both power clocks is 41.625MHz, but the transition time T of the 4-phase power clock is 3ns and the transition time T of the 6-phase power clock is 4ns. The values of corresponding energy consumption (E_{PCH}, E_{PCL}) are also given in Table 1.

4 Conclusions

We have proposed a new power clock system, the 4-phase power clock, for the DSCRL adiabatic circuit. The 4-phase power clock greatly reduces the power clock system's complexity and makes the DSCRL adiabatic circuit easier to be applied. The DSCRL circuit can still keep high efficient energy transfer and recovery driven by the four-phase power clock. The energy dissipation of the DSCRL adiabatic circuit in the four-phase power clock is almost the same as that in the six-phase power clock, which is simulated by the HSPICE with the 0.6μm CMOS technology. Moreover, reducing the number of the power clock can also reduce the energy dissipation in the power clocks circuit system. In fact, the total power dissipation of the DSCRL circuit and the power clock circuit is very low in the four-phase power clock.

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一种用于 DSCRL 绝热电路的新型功率时钟*

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摘要: 提出了一种用于 DSCRL(双摆幅电荷恢复逻辑)绝热电路的新型四相功率时钟, 该功率时钟采用了非对称的方法来优化其时序, 比已提出的采用对称技术来优化时序的六相功率时钟更简洁. 这种新型的功率时钟用于 DSCRL 绝热电路后, 该电路仍然保持了其能量恢复的高效性, 同时还降低了电路设计的复杂性, 这一结论已被文中的 HSPICE 模拟结果证明.

关键词: 能量恢复; 绝热电路; 四相功率时钟

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