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CMOS Dual-Band Low Noise Amplifer

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Abstract: A CMOS dual-band low noise amplifer (LNA) design is presented. The purpose of this work is intended to substitute only one LNA for two individual LNA's in dual-band transceivers for applications such as wireless local area network complying with both IEEE 802.11a and 802.11b/g. Dual-band simultaneous input power and noise matching and load shaping are discussed. The chip is implemented in 0.25μm CMOS mixed and RF process. The measured performance is summarized and discussed.

Key words: low noise amplifier; dual-band receiver; power matching; noise matching; power gain; voltage gain
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1 Introduction

The booming of wireless data communications brings multiple standards for similar applications. IEEE has ratified three standards for wireless local area network(WLAN). Those are IEEE 802.11a, 802.11b, and 802.11g. The newly approved 802.11g standard specifies data rates of up to 54Mbps in the 2.4GHz ISM (industrial, scientific and medical) band. While it uses orthogonal frequency division multiplexing(OFDM), mandatory provisions have been made within the standard to make it inherently compatible with the well-established 802.11b standard at 11Mbps, which uses complementary code keying (CCK) modulation. Both 802.11g and 802.11b operate at ranges of up to 100 meters. The 802.11a standard, which also supports date rates of up to 54Mbps, is designed to operate in the 5-GHz UNII(unlicensed national information infrastructure) band. Although 802.11a and 802.11b use an identical MAC(media access control), 802.11a uses an entirely different encoding scheme called OFDM. The total bandwidth available for 802.11a is 300MHz, which is almost four times that of the ISM band (the ISM band offers only 83MHz of spectrum in the 2.4GHz range). Specifically, 200MHz is at 5.15GHz to 5.35GHz, with the other 100MHz at 5.725GHz to 5.825GHz.

As 802.11a and 802.11b/g operate in different frequency bands with the same application, there are demands for a single chip set to support both of these standards. One possible way is to implement two separate RF front-ends for 2.4 and 5GHz respectively and combine the baseband back-ends. An alternative solution is to design only one RF front-end working at both 2.4 and 5GHz. There are dual-band antenna and filter available. It's possible to design a dual-band LNA working at two frequency bands of interests concurrently and delivering voltage gain[1]. As voltage gain depends on the external load impedance, it is not a comparable figure used to characterize the gain performance of dual-band LNA. In this design S_{21} is used to characterize the power gain performance. Dual-band LNA can serve both bands while dissipating the power as that of the single-band LNA. This choice is an effective solution of power. And dual-band LNA saves a lot of chip area compared to two single-band counter-

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parts. The choice is also a low-cost solution. As 802.11a has two separate wide frequency bands, a dual-band LNA can also be used in this scenario. Dual-band transceiver can work at one band and disable the other to save power at a time, or utilize both bands simultaneously to increase data rate and diversity. Thus it is desirable that dual-band LNA can work at two bands simultaneously.

This paper presents the design of a CMOS dual-band LNA. The prototype of this design was manufactured in 0.25μm silicon based CMOS mixed and RF process. The measured performance of this dual-band LNA is discussed. This work aims at providing dual-band power gain to external 50Ω resistive load used in practical measurement instead of voltage gain to capacitive load[1]. This extends the application of dual-band LNA in superheterodyne architecture.

2 Design of dual-band LNA

The intrinsic transconductance of MOS transistor is inherently wide-band and can be shaped with passive networks to provide gain at dual frequency bands simultaneously.

The simplified schematic of this design is shown in Fig. 1. This topology is preferred to differential one due to power concern and unavailable dual-band balun. The dual-band LNA adopts cascode configuration with inductive source degeneration for its high gain and high isolation between input and output ports, which offers the possibility of achieving the best noise performance of any architecture for single-band LNA[2]. The source degeneration inductor is implemented with bonding wire whose inductance is denoted by L_{dbond}. The dual-band simultaneous input matching is achieved through off-chip parallel resonance tank L_g and C_g, bonding wire L_{bond}, on-chip coupling MIM (metal-insulator-metal) capacitor C_{couple}, intrinsic parasitic capacitance C_{gs} of M1 and down bonding wire L_{dbond}. C_{couple} is used to prevent incoming RF signal from disturbing the operating point of M1.

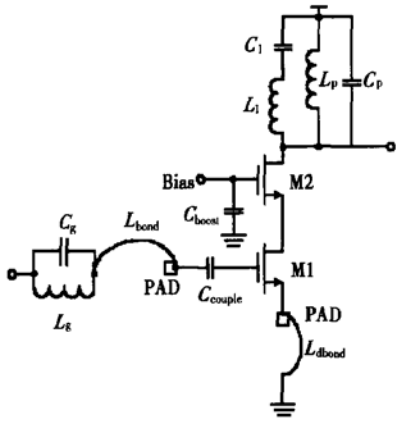

Fig. 1 Simplified schematic of the designed dual-band LNA

Considering the drain noise associated with M1 only, it can be shown that the simultaneous input power and noise matching can be achieved[3]. The components shown in Fig. 1 must satisfy the following equations to achieve this goal

$$\begin{aligned} s(L_{bond}+L_{dbond})+\frac{1}{sC_{couple}}+\frac{1}{sC_{gs}}+\\ \left(sL_g \parallel \frac{1}{sC_g}\right)=0\\ \frac{g_m L_{dbond}}{C_{gs}}=50\Omega \end{aligned} \tag{1}$$

where g_m is the transconductance of M1. From Eq. (1), L_{dbond} can be determined from power matching requirement, M1 and its bias condition. It is clear that there are two frequencies to satisfy Eq. (1), one below and the other above the resonant frequency of LC tank L_g and C_g.

To shape the wide-band transconductance of M1 to provide gain at dual bands simultaneously, the load includes a branch of series resonance tank L_1 and C_1 in addition to conventional parallel LC tank L_p and C_p. The load network will resonate at two distinct frequencies, one below and the other above the resonant frequency of LC tank L_1 and C_1.

If the architecture of dual-band transceiver adopting this kind of dual-band LNA is superheterodyne, to reuse the first stage of the down-conversion mixers the frequency of the first LO (local oscillator) should be chosen with care so

that the image of the lower band signal is located at the notch of the transfer function determined by the series resonance tank L_1 and C_1. As shown in Fig. 2, f_{IL} and f_{IH} are the images of signals f_L and f_H, respectively. To further suppress the image f_{IL}, the resonant frequency of the input parallel resonance tank L_g and C_g is chosen to be the same as that of the tank L_1 and C_1. The image f_{IH} is also suppressed as it is far away from the pass-band of the dual-band LNA.

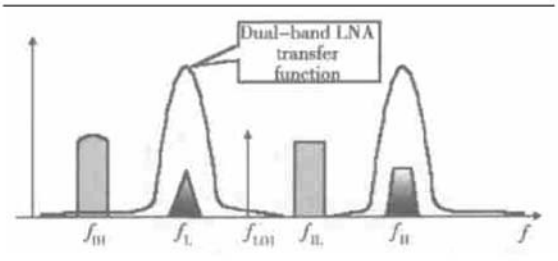

Fig. 2 Frequency-domain representation of the RF signal coming into the dual-band LNA

The capacitance C_{boost} between the gate of cascode transistor M2 and ground is used to boost the gain of the dual-band LNA. As there is intrinsic parasitic capacitance between the gate and the source of the cascode transistor M2, the signal coupling to the gate will degenerate the signal at the output. Adding capacitance C_{boost} will alleviate this effect. The capacitance C_{boost} should be prudently chosen because of input matching and stability considerations.

3 Performance measurement of prototype

The prototype of this design is manufactured in 0.25μm CMOS mixed and RF process. The die photograph of the dual-band LNA is shown in Fig. 3. Due to limited conditions of measurement, the performance of the dual-band LNA cannot be fully measured.

The measured S_{11} and S_{21} of the dual-band LNA are shown in Fig. 4. From the S_{21} curve, it is clear that there are two bands with gain between which there is a notch. The two bands are in the

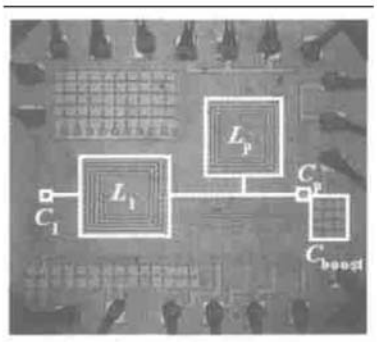

Fig. 3 Die photograph for the dual-band LNA

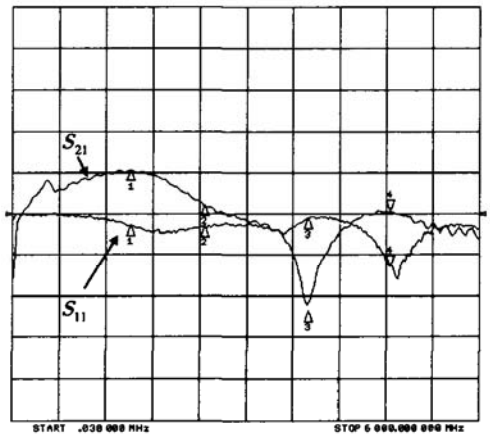

Fig. 4 Measured S_{11} and S_{21} of the dual-band LNA

1.5 ~ 4.8GHz frequency ranges. The S_{21} of the 1.5GHz and 4.8GHz bands are 10.6dB and 1dB, respectively. The frequency of the notch is 3.78GHz. The S_{21} of the notch is - 27dB. It should be mentioned that the measured S-parameters include all off-chip losses such as the losses in bonding wire, PCB (printed circuit board), SMA (subminiature A) connectors, SMA adaptors, and SMA-to-SMA cables. Due to limited conditions of measurement, these losses are not deembeded from the measured S-parameters. The estimation of the overall off-chip loss is 2 ~ 3dB. The S_{11} of the 1.5GHz and 4.8GHz bands are - 3dB and - 13dB, respectively. The input matching of the 4.8GHz band is good enough for this prototype, as there are many factors lacking accurate control such as the length and associated inductance of bonding wires. The best input matching occurs at 5GHz, as the dual-band LNA was designed to work at 2.4 and

5.2GHz bands. The deviation of the measured performance from the simulation is mainly due to the layout and difficulties in parasitic extraction and post-layout simulation. The stringent area requirement was the first consideration in the placement of the two area-consuming spiral inductors, which resulted in the placement of the passive load network marked in the die photograph in Fig. 3. It can be seen from Fig. 3 that there is a long trace to connect L_1 and C_1 series tank to L_P and C_P. The parasitic capacitance and inductance associated with the long trace alter the designed resonant frequencies of the load network. The low power gain of the 5GHz band under good input matching is mainly due to the incapability of the CMOS technology adopted in this design to work at such a high frequency band. The S_{12} of 1.5GHz and 4.8GHz bands are -26.56dB and -22.55dB, respectively. The S_{12} of the notch is -40.37 dB. Based on the measured and simulated S parameters, there are several improvements to make design more accurate. First of all, the accurate modeling of passive and active devices is essential for correct RF circuit design. Judicious layout can minimize parasitic capacitance and inductance associated with the key devices and circuits. Careful post-layout parasitic RLC extraction and simulation can reveal the excursion of performance between the pre- and post-layout design. The performance of the design can be further improved using the post-layout simulation. Cosimulation of silicon and package can predict the performance of RF IC more accurately minimizing the deviation of performance. Deembedding procedure can be used to eliminate the impact introduced by the test fixture and yield the actual characteristics of the DUT (device under test).

As the noise figure analyzer available is Agilent N8973A that supports only up to 3GHz, only the noise figure of the 1.5GHz band is measured. The measured NF of the 1.5GHz is 4dB as shown in Fig. 5. The curves shown in Fig. 5 are the noise figure and power gain of the dual-band LNA. For single-band LNA, the third-order intercept point (IP3) and 1dB compression point(CP1) are used to characterize the linearity performance of single band. These figures of merit are also important for dual-band LNA to characterize the linearity of each band. The measured input CP1 of 1.5GHz and 5GHz bands are 5dBm and 11dBm, respectively. For the same reason mentioned previously, only IP3 for the 1.5GHz band was measured. The measured IIP3 (input third-order intercept point) for 1.5GHz band is 9.7dBm as shown in Fig. 6, which indicates the high linearity of the dual-band LNA.

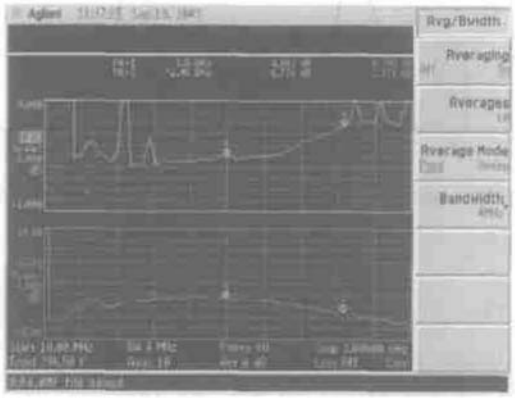

Fig. 5 Measured noise figure of the dual-band LNA from 10MHz to 3GHz

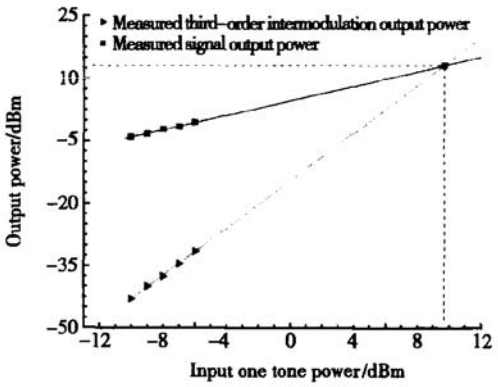

Fig. 6 IP3 of the dual-band LNA in 1.5GHz band

For dual-band LNA, there are other parameters needed to account for the interaction between the two bands in addition to single-band parameters. Cross-band 1 dB compression point and cross-band intercept points can be used to characterize cross-band linearity in addition to single-band linearity figure of merit[3]. A cross-band 1dB com-

pression due to band A is the signal power in band A that causes the small-signal gain in band B to drop 1dB from its nominal value and that will be denoted as $CP1_{A>B}$. A cross-band intercept point has similar meaning to classical single-band intercept point except that the two tones are from different bands. In this design, measurements show that power gain in one band is not affected by the power in other band in the output power range of signal generators used in this measurement. Cross-band intercept points are also unavailable due to limited conditions of measurement.

The measured performance of this dual-band LNA is summarized in Table 1.

Table 1 Measured performance summary of this dual-band LNA

Frequency Band	1.5 GHz	4.8 GHz
S_{21}	10.6 dB	1 dB
S_{11}	- 3 dB	- 13 dB
S_{12}	- 26.56 dB	- 22.55 dB
Input $IP3_{in\text{-}band}$	9.7 dBm	N/A
Input $CP1_{in\text{-}band}$	5 dBm	11 dBm
NF	4 dB	N/A
Notch Suppression	- 27 dB	
Supply Voltage	2.5 V	
DC Current	11.7 mA	
Process	0.25μm CMOS RF Process	
Area	960μm×850μm	

4 Conclusion

The design and measured performance of a CMOS dual-band LNA, which can provide power gain in 1.5GHz and 4.8GHz bands concurrently, are presented. Although the layout has caused deviation of the measured performance from simulation and the dual-band LNA is not fully measured due to the limited conditions of measurement, the measurement shows that the performance of this prototype is promising. The advancement of CMOS technology will provide higher performance transistors, which will improve the performance of this prototype further at higher frequency band. Prudent layout can minimize the deviation between measurement and simulation. This work also demonstrates the availability of power gain from dual-band LNA instead of voltage gain.

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References

[1] Hashemi H, Hajimiri A. Concurrent dual-band CMOS low noise amplifiers and receiver architectures. Symposium on VLSI Circuits Digest of Technical Papers, 2001: 247

[2] Shaeffer D K, Lee T H. A 1.5V, 1.5GHz CMOS low noise amplifier. IEEE J Solid-State Circuits, 1997, 32: 745

[3] Hashemi H, Hajimiri A. Concurrent multiband low-noise amplifiers-theory, design, and applications. IEEE Trans Microw Theory Tech, 2002, 50: 288

CMOS 双带低噪声放大器

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摘要: 描述了基于 CMOS 工艺的双带低噪声放大器的设计, 其目的是用单个低噪声放大器取代双带收发机(如符合 IEEE 802. 11a 和 802. 11b/g 标准的 WLAN) 中的两个单独的低噪声放大器. 讨论了输入功率和噪声的双带同时匹配以及负载对增益的影响. 芯片的加工工艺是 0. 25μm CMOS 混合及射频工艺. 并总结和分析了芯片的测试结果.

关键词: 低噪声放大器; 双带接收机; 功率匹配; 噪声匹配; 功率增益; 电压增益

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