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0.25 m SOI RF nMOSFETs Depleted Partially*

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Abstract: Device structure and fabrication process of SOI nMOSFET depleted partially are proposed for multi-gigahertz RF applications. Many advanced techniques for deep submiron MOSFETs are incorporated into the proposed device. Main steps and conditions in process are given in details, with simulation and optimization by using the process simulator, Tsuprem4. Experiment results of 0.25μm SOI RF nMOSFET are in consistence with simulated ones, and excellent or acceptable parameters of device performance are obtained for multi-gigahertz RF applications.

Key words: structure; process; simulation; experiment; silicon on insulator; radio frequency
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1 Introduction

Recently, the scaling-down of CMOS has resulted in a significant improvement in the RF performance of MOS devices. Consequently, CMOS has become a viable option for analog/RF applications and RF system-on-a-chip (SOC) in multi-gigahertz applications. CMOS technology has superiorities in mature process, low cost, and high integration density when compared with GaAs technology, which is widely used in RF applications. On the other hand, bulk silicon substrates suffer from higher loss and inferior isolation, and passive devices with high quality factor are very difficult to integrate into such substrates. Thanks to the isolation of buried oxide (BOX) layer, SOI devices exhibits higher speed, and can partially overcome the aforementioned issues, thus they are becoming increasingly important in the RF research field[1,2].

The emphasis of previous work was on the values of the RF parameters, but balanced DC parameters were often neglected, and detailed steps in process were seldom mentioned. However, for RF-IC applications, DC characteristics are still important. This paper describes detailed process of 0.25μm SOI RF nMOSFET depleted partially, which was validated by a process simulator before device fabrication, and the device experiment exhibits excellent or acceptable DC and RF performance.

2 Device fabrication

The 0.25μm gate length RF MOSFETs were fabricated on SIMOX wafers from Ibis Tech. Corp., with material parameters as followings: p(100), 15~25Ω·cm, 198nm silicon film, and 382nm buried oxide layer. Main processes were based on the technology platform for 0.1~0.35μm CMOS integrated circuit developed in the Institute of Microelectronics, the Chinese Academy of Sci-

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ences (IMECAS)[3,4], and some necessary adjustments were adopted for SOI process. The main steps in process are shown in Table 1.

Table 1 Main steps in process for the fabrication of 0.25μm SOI RF nMOSFETS

Step	Condition
Field oxidation (LOCOS)	450nm
Pre-oxidation	15nm
Threshold adjusting implantation	BF_2, 80keV, 2×10^{12} cm^{-2}
Anti-punchthrough implantation	B, 70keV, $4\times10^{13}cm^{-2}$
Nitrided gate oxidation	5.5nm
LPCVD poly-Si	300nm
Poly patterned with E-Beam direct-writing	JEOL JBX-5000LS tool, SAL-601 photoresist
TEOS SiO_2 for sidewall 1	30nm
Extension implantation	As, 5keV, $3.5\times10^{14}cm^{-2}$
TEOS SiO_2 for sidewall 2	250nm
S/D implantation	As, 50keV, $4\times10^{15}cm^{-2}$
Body-contact implantation	BF_2, 40keV, $5\times10^{15}cm^{-3}$
RTA	1015℃, 6s
Pre-amorphous implantation	Ge, 40keV, $3\times10^{14}cm^{-3}$
Ti sputtering	Ti, 25nm
RTA	670℃, 5s
Selective etching	
RTA	880℃, 10s
Dual-layer-metallization	TiN/AlSi/TiN/Ti
Passivation	

Since it provided excellent resolution but took much time, E-beam direct-writing was only used in poly-Si gate pattern, and I-line optical lithography was used in other layers, considering the trade-off between precision and efficiency. Dual implants (B and BF_2) were used in channel engineering to form retrograde doping profile for adjustment of threshold voltage and minimization of short-channel effects (SCE). Then, E-beam direct-writing technique combined with wafer pretreatment in plasma of CF_4 was the key factor of 0.25μm poly-silicon gate pattern. Shallow extension junction of source/drain (S/D) with high enough doping was requested for slight SCE and low series S/D resistance, which were acquired by combining low energy As implanting with rapid thermal annealing (RTA). Ti-salicide with Ge pre-amorphous implant (PAI) is used to maximally minimize the parasitical resistance of gate, drain, and source electrodes. For the layout structures, the multi-finger gate pattern was used to reduce the gate parasitical resistance. The body-contact structure, by using the p-type implant beside the channel, was employed to restraint floating-body-effects, and the floating-body device was also fabricated for comparison. Planar spiral inductors and metal-insulator-metal (MIM) capacitors, which are important for RFIC, can also be introduced into circuits by the following dual Al layers. Before experiments, all steps in process shown in Table 1 were simulated and optimized by using Tsuprem4[5], a two-dimensional numeric simulator for semiconductor process.

3 Results and discussion

The SEM micrograph in Fig. 1 shows the cross section of 0.25μm poly-Si gate, whose etching profile is strictly anisotropic and smooth. The simulated doping information is shown in Fig. 2 including the doping profile of the channel, the extension, and the S/D regions. The y-axis is net im-

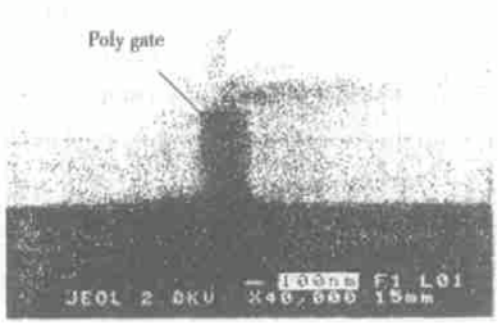

Fig. 1 Cross section of SEM micrograph for 0.25μm poly-Si gate

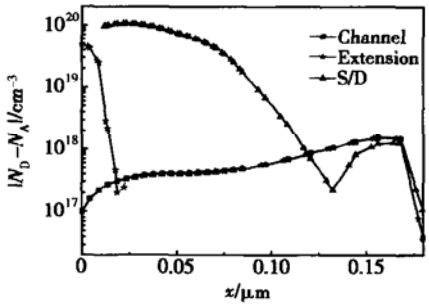

Fig. 2 Simulated net doping profile along the distance

purity concentration, i.e., the donor impurity concentration minus the acceptor impurity concentration, while the x-axis is distance from the Si/SiO_2 interface. The S/D junction depth(x_j) is 130nm or so, while the extension is very shallow but its surface is highly doped with a value of 5×10^{19} cm^{-3} (N_{ext}), which agrees well with measurement results in Table 2. And the channel doping profile is retrograde as expected.

Table 2 Simulated and experimental results of structure and performance parameters of body-contact SOI RF nMOSFET devices

Parameter	t_{TSi_2} /nm	x_j /nm	N_{ext}/ cm^{-3}	R_n/ ($\Omega\cdot\square^{-1}$)	R_p/ ($\Omega\cdot\square^{-1}$)	V_{th}/ ($\Omega\cdot\square^{-1}$)	g_m/ ($mS\cdot nm^{-1}$)	I_{off}/ ($nA\cdot\mu m^{-1}$)
Simulation	17	133	4.9×10^{19}	6.5	7.1	0.51	–	–
Measurement	32	117	5.0×10^{19}	5~6	6~7	0.4~0.45	195	< 0.05[1)]

1) Less than the noise current of the probe setup

The output characteristics of SOI body-contact(BC) nMOSFET are shown in Fig. 3(a), while Figure 3(b) depicts those of floating-body(FB) device for the purpose of contrast. The FB nMOSFET exhibits distinct kink effect even when V_G is low as 1V; however, the BC device only begins to show slight kink effect with relatively high V_G and V_D, but more insignificant when compared with that of the FB device. For BC device, floating-body effects are unable to avoid completely because the channel are so wide (10μm per finger) that the effect of body-contact is weakened by the resistance across the channel. Nevertheless, the curves shown in Fig. 3(a) are acceptable by and large. The transfer characteristics are shown in Fig. 4. From the two curves with V_D bias of 0.1V and 2V, some DC parameters can be extracted: V_{th} = 0.45V, S = 84mV/decade, V_{DIBL}= $\Delta V_{th}/\Delta V_D$= 75mV/V, and I_{off} < 0.05nA/μm. All of these parameters are excellent and comparable with previous literatures[3,4]. Some other parameters are also summarized in Table 2, and both simulation and measured results are given by contrast. Acceptable consistence between simulation and measurement has been achieved except for the discrepancy of the $TiSi_2$ thickness: the measurement result (32nm) is much thicker than the simulation one (17nm), and it is presumably because the time of actual RTA process was longer than that of simulation due to the rise-time and fall-time of temperature.

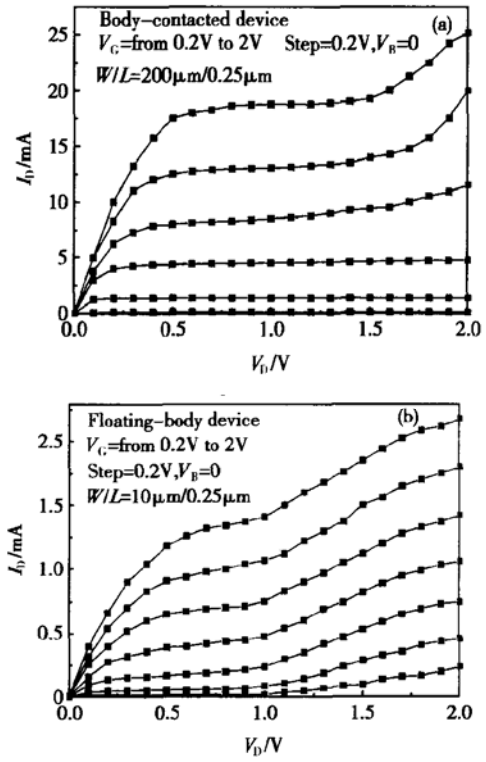

Fig. 3 Output characteristics of SOIRF nMOSFETs (a) Body-contact-device; (b) Floating-body-device

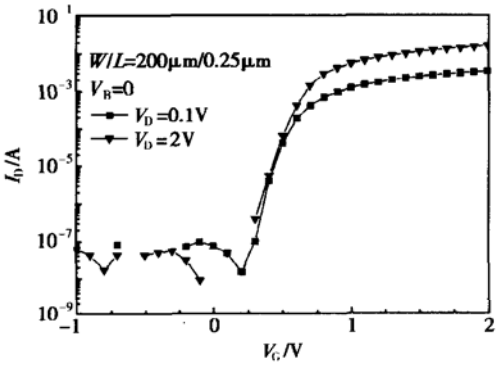

Fig. 4 Transfer characteristics of SOI RF nMOSFET

The saturated transconductance extracted from Fig. 3(a) is 195mS/mm, which is excellent for 2V bias. Then, the extrapolated cutoff frequency

(f_T) and maximal oscillation frequency (f_{max}) are also acquired from Fig. 5. After the de-embedding approach, f_T is 17.78GHz and f_{max} is 15.03GHz, respectively. Of course, these values are not very high, possibly because of the Al-metallization, the low-resistivity substrate and the parasitical capacitance resulted from the lateral body-contact structure[6,7], but they are competent for multi-gigahertz RF applications.

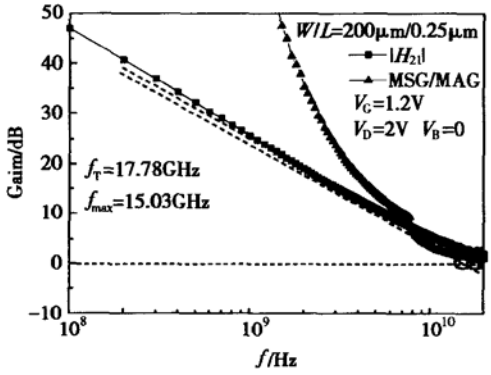

Fig. 5 Gain curves of SOI RF nMOSFET

4 Conclusion

In this paper, structure and process of SOI nMOSFET, compatible with Si CMOS technology, have been proposed for multi-gigahertz RF application. Process steps and conditions were given in details after simulation and optimization by Tsuprem4, and 0.25μm SOI RF nMOSFETs were fabricated. The measured structure parameters are in consistence with simulated ones, and the body-contact nMOSFET exhibits excellent DC characteristics and acceptable RF performance. Such structure and process of SOI nMOSFET are feasible for multi-gigahertz RF applications.

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部分耗尽 0.25 m SOI 射频 nMOSFET*

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摘要：结合多项用于深亚微米集成电路的新技术，提出了用于数 GHz 射频集成电路的 SOI nMOSFET 器件结构和制造工艺. 经过半导体工艺模拟软件 Tsuprem4 仿真和优化，给出了主要的工艺步骤和详细的工艺条件. 制作了 0.25μm SOI 射频 nMOSFET 器件，结构和工艺参数同仿真结果一致，测试获得了优良的或可接受的直流及射频性能.

关键词：结构；工艺；仿真；实验；射频；SOI

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