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An Improved Description of Characteristics Length in Substrate Current Model for Submicron and Deep-Submicron LDD MOSFET's*

Yu Chunli, Yang Lin'an and Hao Yue

(*Microelectronics Institute, Xidian University, Xi'an 710071, China*)

Abstract: A novel substrate current model is proposed for submicron and deep-submicron lightly-doped-drain (LDD) n-MOSFET, with the emphasis on accurate description of the characteristics length by taking the effects of channel length and bias into account. This is due to that the characteristics lenth significantly affects the maximum lateral electric field and the length of velocity saturation region, both of which are very important in modeling the drain current and the substrate current. The comparison between simulations and experiments shows a good prediction of the model for submicron and deep-submicron LDD MOSFET. Moreover, the analytical model is suitable for descgn of devices as it is low in computation consumption.

Key words: LDD MOSFET; substrate current; characteristics length; maximum lateral electric field
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1 Introduction

Substrate current is a very sensitive parameter to monitoring the hot carrier degradation in scaling down devices to deep submicron. The lightly-doped-drain (LDD) process technology finds wide applications in the improvement of hot carrier immunity. However, the substrate current in LDD MOSFET still demonstrates a unique characteristics different from the conventional MOSFET, particularly in very short gate length devices. The modeling of substrate current for LDD structure is therefore different from that for conventional S/D structure devices. Many publications in this area have given a great deal of experiments and analysis[1~5], nevertheless, lack of clear differences in modeling mechanism between LDD and conventional S/D structures. In details, the modeling of n^- doped region induced effective channel length, the modeling of velocity saturation region length, the modeling of threshold voltage and saturation voltage, etc., should be paid more attention to LDD structure. References[3~5] demonstrate the improved substrate current models, but not especially for LDD devices.

In this paper we investigate the mechanism of the substrate current of LDD MOSFET, and put

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Yu Chunli female, PhD candidate. Her research interests focus on the reliability and modeling of deep-submicron devices.

Yang Lin'an male, PhD. His research interests include reliability of deep-submicron devices and modeling & fabrication of microwave power devices based on wide band gap semiconductor materials.

Hao Yue male, professor. His research interests include IC reliabilit, manufacturability, methodology for IC design, and new type of semiconductor devices and circuits.

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the emphasis on the modification of the characteristics length which is also defined as the effective ionization length in some papers. The characteristic length significantly affects the modeling of drain current and substrate current for the MOSFET from long channel to short channel. Thus many papers have to utilize the extracted empirical descriptions to pursue the model accuracy. To this end, a modified characteristics length model of LDD MOSFET is developed which is suitable for the description of submicron and deep-submicron devices, and is implemented in the proposed drain current and substrate current models. The related experiments are compared with the simulation results as validity.

2 Improved model of characteristics length

An accurate description of maximum lateral electric field E_m is extremely important for calculating the substrate current. From quasi two-dimensional simulation, E_m is given as[6]

$$E_m = \sqrt{\left[\frac{V_{ds} - V_{dsat}}{l}\right]^2 + E_c^2} \tag{1}$$

where V_{dsat} and E_c are saturation voltage and critical saturation electric field, respectively. If the critical saturation electric field E_c is neglected, it is simplified to Eq. (2) which is widely used in modeling substrate current shown as

$$E_m \approx \frac{V_{ds} - \eta V_{dsat}}{l} \tag{2}$$

where l is defined as the characteristics length (or effective ionization length), a very important parameter in modeling the maximum electric field. The emphasis in this paper is in turn put on the description of characteristics length for the MOSFETs with different gate lengths and structures. η is an adjustable parameter close to unity to fit the experiment.

In solving the distribution of channel electric field, the parameter l is normally defined as

$$l = \sqrt{\frac{\epsilon_{si}}{\epsilon_{ox}} t_{ox} x_j} \tag{3}$$

where t_{ox} and x_j are the gate oxide thickness and the S/D junction depth (n^- region junction depth for LDD MOSFET), respectively. However, this expression yields a significant dispersion as the LDD device is scaled down to submicron or deep-submicron regime. Many experiment-based modification methodologies therefore have been developed to improve the model accuracy. Some empirical expressions are given as follows[7]:

$$l = 0.0007 x_j^{1/3} t_{ox} \tag{4}$$

where x_j and l are in micrometers, t_{ox} is in angstroms. It is suitable for short channel length LDD or conventional MOSFET.

$$l = 0.22 x_j^{1/2} t_{ox}^{1/3}\text{[8]} \tag{5}$$

where l, x_j, and t_{ox} are in centimeters. Equation (4) is suitable for long channel devices, although occasionally being used in submicron devices.

In practice, the parameter l is gate bias- and drain bias-dependent. Thus an empirical bias-dependent model is developed as[9]

$$l = l_0 + l_1(V_{ds} - V_{dsat}) + l_2(V_{ds} - V_{dsat})^2 \tag{6}$$

where l_0, l_1, and l_2 are fitting parameters. Furthermore, the third order is even considered in some fitting models.

The measurements of E_m against V_{gs} and V_{ds}[1,2] demonstrate that E_m is approximately proportional to V_{ds} and inversely proportional to V_{gs}, and also l is approximately proportional to V_{gs} in short gate length LDD MOSFET's. The parameter l affects not only the maximum lateral electric field, but also the threshold voltage V_{th}. In this paper, we develop an equivalent model of characteristics length l which takes the bias and the channel length into account, universally suitable for submicron and deep-submicron regiem, given as

$$l = l_0[a_1 L_{eff}^{1/5} + a_2 V_{gs}(V_{ds} - V_{dsat})^2] \tag{7}$$

where l_0 and L_{eff} are in micrometers, defined as the effective characteristics length and the effective channel length of submicron and deep-submicron LDD MOSFET, respectively. l_0 is given by Eq. (4)

which holds the accuracy in short channel LDD devices. The first term in the square bracket of Eq. (7) indicates that l is related to the gate length. Experimentally, the characteristics length l increases nonlinearly as the gate length increases. From submicron to deep-submicron regime, the change is not apparent, and the gate length-independent empirical model is in turn well used. In the micron regime, the difference of l is larger. This can also be evidenced by Eqs. (3), (4), and (5). Thus the exponent 1/5 is proposed to fit the effect of gate length on the characteristics length l in a wide range from micron to deep-submicron. The second term in the square bracket of Eq. (7) indicates that the practical characteristics length l is nearly proportional to the gate bias[7]. The drain bias-dependent factor is also considered in this term in which the square factor is close to the reality. a_1 (μm^{-1}) and a_2 (V^{-3}) are fitting parameters. Then, this model is implemented in l_d and V_{th}[10], to model the substrate current of the LDD MOSFET from submicron to deep submicron regime.

3 Modeling of substrate current for LDD MOSFET's

Theoretically, the formations of substrate current I_{sub} are of less difference between conventional S/D and LDD MOSFET's. The key consideration of I_{sub} model for LDD MOSFET is in both modeling of I-V characteristics in which the parameters such as parasitic series resistance, effective channel length, and threshold voltage shift, etc., are included for LDD technology and implementation of I_{sub}. The commonly used description of substrate current I_{sub} taking the Eq. (2) into account is given by[9]

$$I_{sub} = I_{ds} \times \frac{A_i}{B_i}(V_{ds} - \eta V_{dsat}) \exp\left(- \frac{lB_i}{V_{ds} - \eta V_{dsat}} \right) \quad (8)$$

where I_{ds} and V_{dsat} are drain current, saturation voltage, respectively, and A_i, B_i are impact ionization coefficients. The differences among many I_{sub} models are in differences of the parameters V_{dsat}, l and E_m, etc. With appropriate determination of these parameters for LDD MOSFET, the I_{sub} model can be used to demonstrate the hot carrier effects. The saturation voltage V_{dsat} is obtained by

$$V_{dsat} = L_{eff}E_c \left[\sqrt{1 + \frac{2(V_{gs} - V_{th})}{\gamma L_{eff}E_c}} - 1 \right] \quad (9)$$

where the effective channel length L_{eff}, the bulk charge factor γ, and the critical saturation electric field E_c are shown in Refs. [11, 12].

A hyperbolic-tangent description has been developed to characterize the drain current I_{ds} for LDD MOSFET's[13]:

$$I_{ds}(V_{gs}, V_{ds}) = I_{dsat}(1 + \lambda V_{ds}) \mathrm{th}(\alpha V_{ds}) \quad (10)$$

where I_{dsat}, α and λ are critical saturated drain current, saturation voltage parameter, and channel length modulation parameter, respectively. Taking the effect of source and drain parasitic resistances (these parasitic parameters are normally extracted from experiments rather than calculations because of their complicity for LDD MOS structure) into account, the iteration methodology is used to solve the nonlinear function Eq. (10) where the Gauss Newton and the Levenberg Marquardt optimization algorisms are utilized.

4 Simulation results of I_{sub} model and validity

All the proposed parameters are implemented in the model to simulate the characteristics of short gate length of LDD NMOSFETs and the results are compared with the experiments. Figure 1 shows the substrate current of W/L_{eff} = 55μm/0.62μm LDD MOSFET, in which the gate oxide thickness t_{ox} equals 25nm, the junction depth of n^- region x_j equals 0.25μm, the extracted source and drain parasitic resistances equal 11.27Ω and the n^- region and the channel region under the gate oxide of substrate are $N_D = 1.0\times10^{18}cm^{-3}$ and $N_A = 4.08\times10^{16}cm^{-3}$, the flat band voltage $V_{FB} = -0.6V$, the electron mobility in the channel $\mu_s = 604.88cm^2/(V \cdot s)$, respectively[1]. The comparison between the ex-

periment and the simulation illustrates a good prediction of this improved substrate model. As validity, the output drain current calculated from the model including the effect of substrate current given in Fig. 2, showing an excellent agreement be-

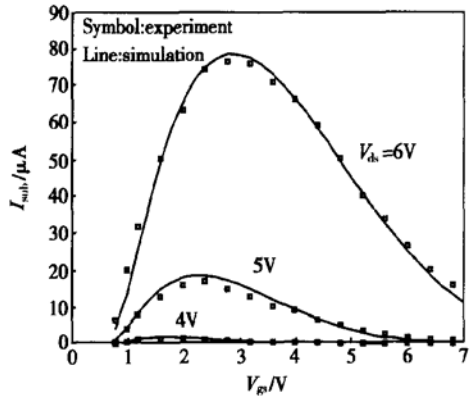

Fig. 1 Simulation and experiment of substrate current versus gate bias for LDD MOSFET with 0.62μm effective channel length at V_{sb}= 0V

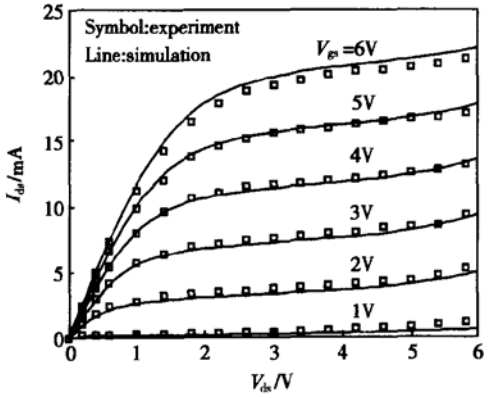

Fig. 2 Simulated and experimental I_{ds}-V_{ds} characteristics of L_{eff}= 0.62μm LDD MOSFET

tween measurement and simulation. The simulated drain conductance is given in Fig. 3 simultaneously, showing a smooth transition between linear region and saturation region, and the effect of substrate current on the drain current at large drain bias region. In this paper, the extracted parameters for substrate current simulation are given as: B_i= 1.92×10^6V/cm is treated as a fixed value which is calculated from the properties of bulk silicon[9], A_i = 0.4×10^6 cm^{-1}, a_1= 1.15μm^{-1}, a_2= 1.8×10^{-3} V^{-3}, η= 1.05. Moreover, a micron LDD NMOSFET with L_{eff}= 1.02μm is simulated by this model in Figs. 4, 5, and 6 which show the substrate current, the output I-V characteristics, and the drain

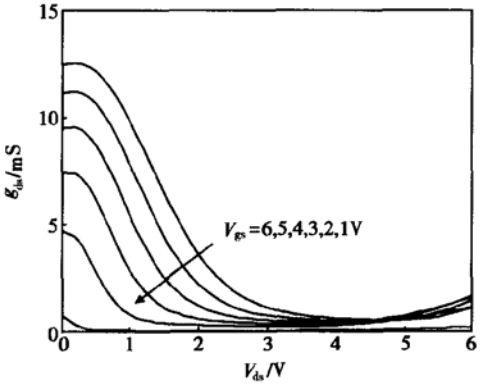

Fig. 3 Simulated drain conductance of the W/L_{eff}= 55μm/0.62μm LDD MOSFET

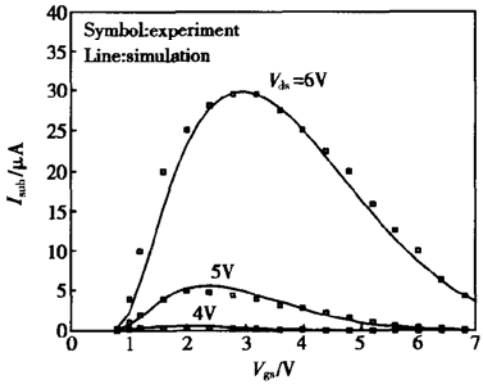

Fig. 4 Simulation and experiment of substrate current versus gate bias for LDD MOSFET with 1.02μm effective channel length at V_{sb}= 0V

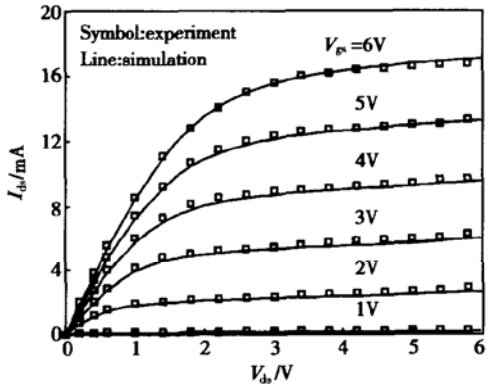

Fig. 5 Simulated and experimental I_{ds}-V_{ds} characteristics of L_{eff}= 1.02μm LDD MOSFET

conductance, respectively. The same extracted pa-

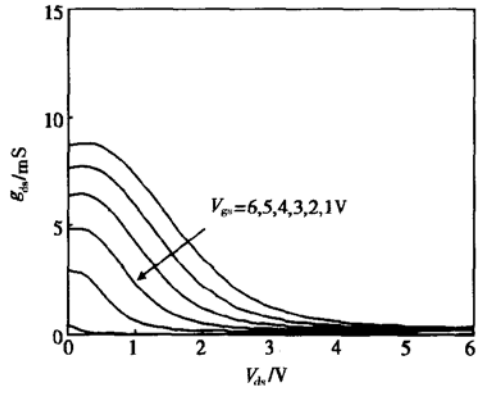

Fig. 6 Simulated drain conductance of the L_{eff} = 1.02μm LDD MOSFET The effect of substrate current at large drain bias region are very small.

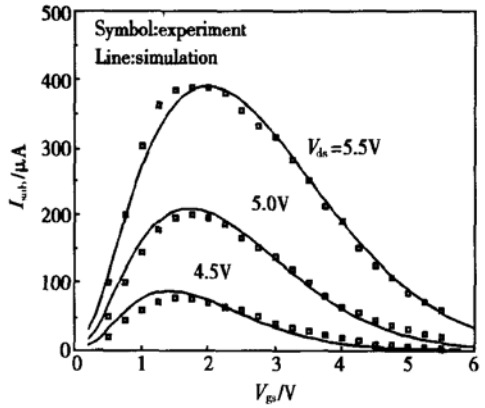

Fig. 7 Simulation and experiment of substrate current versus gate bias for W/L_{eff} = 40μm/0.32μm LDD MOSFET, where the substrate bias V_{sb} = 0V. A large increase of I_{sub} is shown compared with that in Figs. 1 and 4.

rameters are used except the drain voltage adjustable parameter η = 0.95. All the simulations demonstrate satisfying predictions to the reality of LDD MOSFETs, therefore presenting the robustness of the model although the effective channel length of 1.02μm is beyond the submicron regime. It is also obvious that the long gate length MOSFET gives rise to the low substrate current. This is the reason that the study on the mechanism of substrate current is important for submicron and deep-submicron devices in the reliability area. Simultaneously, the performance of a LDD MOSFET with shorter gate length (W/L_{eff} = 40μm/0.32μm) is simulated by the model. Figure 7 shows the comparison between measurement[14] and simulation of the substrate current, resulting in good agreement. The calculated I_{ds}-V_{gs} curves from the linear region to saturation region are drawn in Fig. 8 with the experimental data (at V_{ds} = 5V) as comparison. The utilized parameters in simulations are: t_{ox} = 15nm, x_j = 0.25μm, N_A = 6.2$\times 10^{16}$ cm^{-3}, N_D = 1$\times 10^{18}$ cm^{-3}, $R_S(R_d) \approx 30\Omega$, μ_s = 600cm^2/(V·s), V_{FB} = −0.87V, etc. The extracted parameters for substrate current simulation are given as: A_i = 0.38$\times 10^6$cm^{-1}, B_i = 1.92$\times 10^6$V/cm, a_1 and a_2 maintain the same value as mentioned above in extraction and equal 1.15 and 1.8$\times 10^{-3}$, and η = 1.06 respectively. Further more, a very short gate length's LDD NMOSFET (W/L_{mask} = 20μm/0.26μm) fabri-

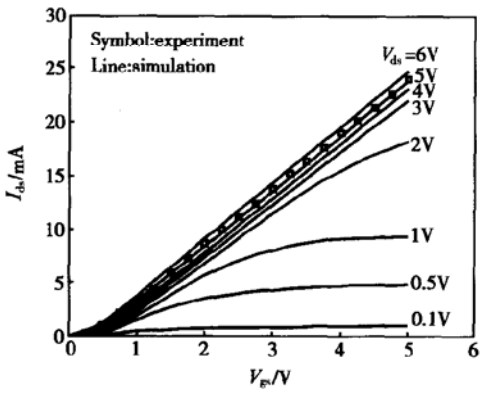

Fig. 8 Comparison between simulated I_{ds}-V_{gs} characteristics from linear to saturation region and measurement

cated on 0.18μm CMOS technology is also investigated, and the good results shown in Figs. 9 and 10 are obtained. The extracted parameters by linear regression method in simulations are: t_{ox} = 3.2nm, L_{eff} = 0.23μm, x_j = 0.03μm, N_A = 3$\times 10^{16}$cm^{-3}, N_D = 1.1$\times 10^{18}$cm^{-3}, $R_S(R_d) \approx 14.5\Omega$, μ_s = 750cm^2/(V·s), V_{th} = 0.48V, etc. The extracted parameters for substrate current simulation are given as: A_i = 0.21$\times 10^6$cm^{-1}, B_i = 1.92$\times 10^6$V/cm, a_1 and a_2 maintain the same value as mentioned above in extraction and equal 1.15 and 1.8$\times 10^{-3}$, and η = 1.15, respectively. All of these investigations indicate that the improved model is suitable for the

LDD MOSFETs of a large region of gate lengths with low difference of extractions.

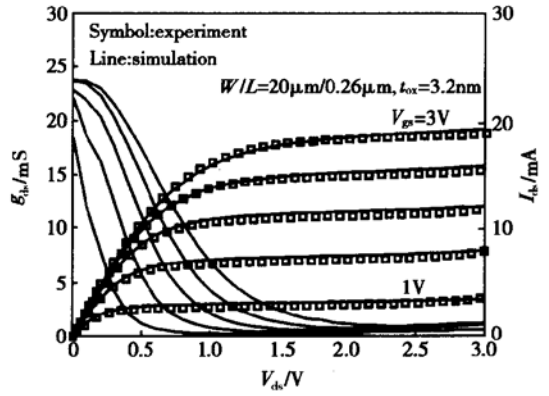

Fig. 9 Simulated and experimental substrate currents in 0.26μm gate length LDD NMOSFET ($L_{eff} \approx$ 0.23μm)

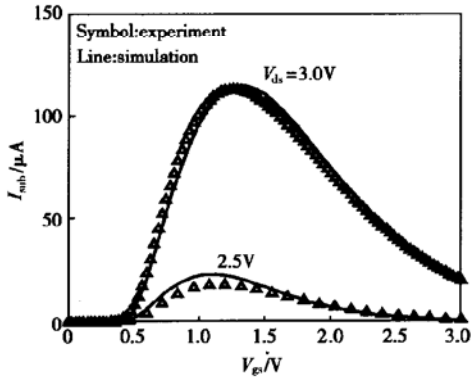

Fig. 10 Simulated and experimental output drain current and drain conductance in 0.26μm gate length LDD NMOSFET

5 Conclusion

We have proposed a new description of ionization characteristics length l which is relevant to effective channel length and bias. With the improved parameter, the substrate current model and I-V characteristics model is developed to predict the performance of submicron and deep-submicron LDD n-MOSFETs. The comparison between measurements and simulations shows good agreement. Furthermore, this analytically-based model possesses an advantage of very low calculation consumption over the numerical model, suitable for the practical design of devices.

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亚微米、深亚微米 LDD MOSFET 的衬底电流模型中特征长度改进的描述*

于春利 杨林安 郝 跃

(西安电子科技大学微电子研究所, 西安 710071)

摘要: 建立了衬底电流模型中特征长度参数的改进描述, 该参数的引入使衬底电流模型能够有效地适用于从微米尺寸到亚微米、深亚微米尺寸的 LDD MOSFET. 在以双曲正切函数描述的 I-V 特性基础上, 该解析模型的运算量远低于基于数值分析的物理模型, 其中提取参数的运用也大大提高了模型的精度, 模拟结果与实验数据有很好的一致性.

关键词: 轻掺杂漏 MOSFET; 衬底电流; 特征长度; 最大横向电场

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于春利 女, 博士研究生, 从事深亚微米 CMOS 器件建模及可靠性应用的研究.

杨林安 男, 博士, 研究方向为小尺寸微波器件、宽禁带半导体材料和器件领域.

郝 跃 男, 教授, 博士生导师, 从事微电子学与半导体器件的研究.

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