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High Temperature Characteristics of 3C-SiC/Si Heterojunction Diodes Grown by LPCVD*

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Abstract: The high temperature (300~ 480K) characteristics of the n-3C-SiC/p-Si heterojunction diodes (HJD) fabricated by low-pressure chemical vapor deposition on Si (100) substrates are investigated. The obtained diode with best rectifying properties has 1.8×10^4 of ratio at room temperature, and slightly rectifying characteristics with 3.1 of rectification ratio is measured at 480K of an ambient temperature. 220V of reverse breakdown voltage is acquired at 300K. Capacitance-voltage characteristics show that the abrupt junction model is applicable to the SiC/Si HJD structure and the built-in voltage is 0.75V. An ingenious equation is employed to perfectly simulate and explain the forward current density-voltage data measured at various temperatures. The 3C-SiC/Si HJD represents a promising approach for the fabrication of high quality heterojunction devices such as SiC-emitter heterojunction bipolar transistors.

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1 Introduction

Silicon carbide (SiC) has been largely investigated in last years because of its outstanding physical properties (wide band gap, high thermal conductivity, and high saturated electron drift velocity) that make it a superior material for high power and high-temperature electronics[1]. Although over 250 one-dimensional SiC polytypes exist[2], there is only one repetitive ABC stacking sequence yielding a zincblende structure, referred to as 3C-SiC or β-SiC. Since cubic 3C-SiC is metastable and therefore difficult to grow in large bulk form, it has been heteroepitaxially grown typically on silicon substrates at 1000~ 1400℃ using conventional chemical vapor deposition (CVD)[3~5]. The 3C-SiC-Si system has certain attractive applications. The first is in the field of robust sensors operating at high temperatures and harsh environments. The second is in the field of low-cost large area substrates for the nitride epitaxy. The third is the development of semiconductor devices for the post CMOS era in silicon ultra large scale technology. In particular. the SiC/Si

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heterostructures are of considerable interest in realizing wide-band-gap emitters or window regions in bipolar transistors[6], photodetectors[7], and electroluminescent devices[8]. Since the bandgap of SiC is wider than that of Si, a valence-band discontinuity (ΔE_v) at the interface of n-p SiC/Si heterojunction diminishes the injection of holes from Si into SiC. As a result, the emitter efficiency in an n-p-n SiC/Si/Si HBT is high, even if the doping level of the base layer is fairly high[9,10].

However, beneath the fundamental problem of heteroepitaxial growth in the material system with large lattice mismatch (20%) and thermal misfit (8%) between Si and cubic β-SiC, voids in the shape of inverted pyramids are often formed in Si substrate surfaces during the growth of SiC by Si out-diffusion at high temperature, which significantly affects the electrical properties of SiC/Si heterojunctions[11,12]. Although several groups have opened up SiC/Si heterojunction devices such as HJD and HBT[13,14], the breakdown voltage of which is not very high. In previous works[15~20], the author's group made efforts to improve the epitaxy of 3C-SiC on Si substrates and reported on the LPCVD growth of voids-free n-3C-SiC/p-Si and the preliminary heterojunction characteristics. In this paper, n-3C-SiC/p-Si HJD with good electrical properties is obtained and the characteristics of the HJD at various temperatures ranged from 300 to 480K are investigated. An ingenious equation is presented to simulate and explain the forward current density-voltage (J-V) data measured at different temperatures and thus the electrical transport properties are discussed. The 3C-SiC/Si HJD represents a promising approach for the fabrication of high quality HJ devices such as SiC-emitter HBT.

2 Experiment

The 3C-SiC/Si heterojunction diodes were fabricated by growing unintentionally doped 3C-SiC on 10~ 12 Ω·cm p-type Si (100) substrates using a horizontal LPCVD system. SiH_4, C_2H_4, and Pd-cell purified H_2 were used as precursor gases. The ultrasonically cleaned, chemically treated, finally dried Si substrates were subjected to a pregrowth etch in hydrogen at about 1200℃ for 10min to remove any trace of contamination and produce a surface suitable for carbonization and subsequent epitaxy. The flow rates of SiH_4, C_2H_4, and H_2 were 1, 5, and 3000sccm, respectively. The SiC layers were grown at 1300℃ under low pressures (2.6×10^4Pa). In order to prevent the formation of voids and to obtain improved interface of 3C-SiC/Si, much attention has been paid to the pretreatment and carbonization process of the substrates. Further details of the LPCVD growth and of the diode's fabrication process have been published earlier[15~20]. The thickness, carrier concentration, and Hall mobility of 3C-SiC layer is 1~ 2μm, $1.4\times10^{17}cm^{-3}$, 690 $cm^2/(V\cdot s)$. Al was sputter deposited on both sides with 200nm of thickness. The area of the HJD's is about 1mm×1 mm, which was obtained by cleaving along ⟨10⟩ direction. Then the capacitance-voltage (C-V) and current density-voltage (I-V) characteristics of the HJD were measured by HP4284A and HP4140B meters, respectively.

3 Results and discussion

3.1 Room temperature J-V characteristics

The room temperature J-V characteristics of the SiC/Si HJD are plotted in Fig. 1(a). The diode rectification ratio of forward to reverse (commonly defined at ±1V bias) is 3.8×10^3. And the diode with best rectifying properties we obtained has 1.8×10^4 of ratio. The deviation from linearity at high forward current is due to a series resistance associated with ohmic contacts and body resistance. The reverse current increases gradually with increasing reverse bias. Leakage current densities are measured at 1.0 and 3.0V reverse bias to be 1.81×10^{-4} A/cm^2 and 3.57×10^{-4} A/cm^2, respectively. Most of the diodes we obtained exhibit over 100V of reverse breakdown voltage (here not shown), and the best diode has approximately 220V of hard breakdown voltage. Figure 1(b) shows a $1/C^2$-V plot of a SiC/Si heterojunction diode. The C-V data are measured at 100kHz of frequency at room temperature. The $1/C^2$ versus V data of Fig. 1(b) reveals a linear relationship indicating that the SiC/Si HJD structure has abrupt junction. As can be seen, the built-in voltage V_{bi} is 0.75V.

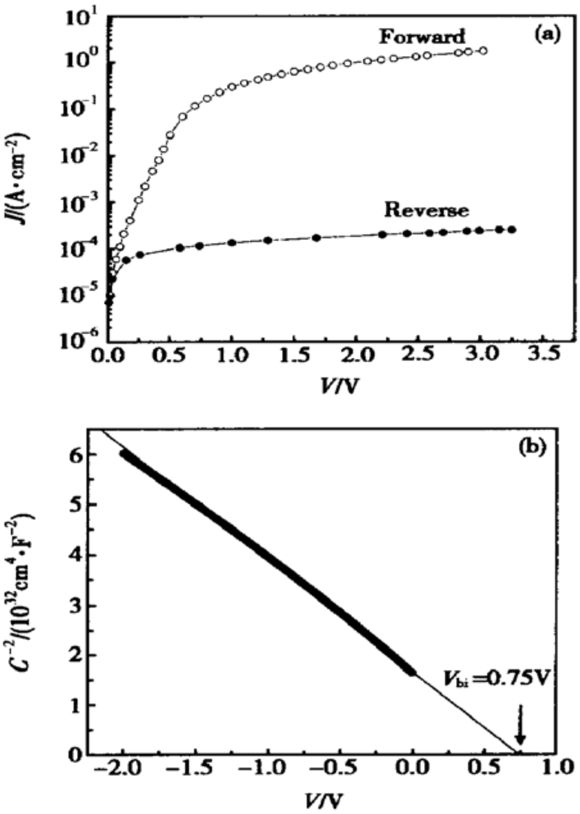

Fig. 1　J-V (a) and C-V (b) characteristics of the SiC/Si heterojunction diode at room temperature

3.2　High temperature J-V characteristics

Figire 2 shows the J-V characteristics of the n-p heterojunction diode measured at four different temperatures, 300, 340, 430, and 480K. As expected, the increase in temperature caused an increase in leakage current and a decrease in the effective breakdown voltage (here not shown). The temperature effect of the HJD indicates that the junction breakdown has a negative temperature coefficient, which is dominated by the tunneling mechanism[21]. At 340K and 430K, the rectification ratio decreases to 174 and 13 respectively. Slightly rectifying characteristics with 3.1 of rectification ratio were measured at 480K of ambient temperature.

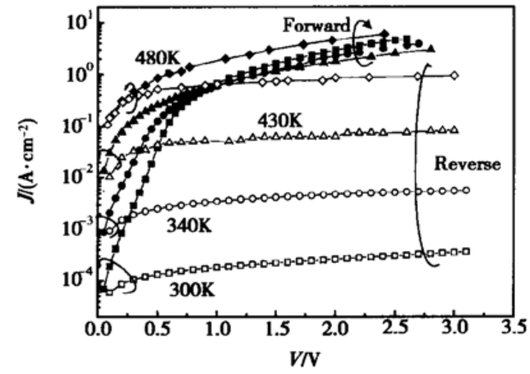

Fig. 2　J-V characteristics of the SiC/Si heterojunction diode at different temperatures

As can be seen from Fig. 2, at low current densities $J <$ 0.8A/cm^2, the voltage drop across the diode decreases with increasing temperature owing to the reduction of the built-in potential. By contrast, at high current densities $J >$ 0.8A/cm^2, the voltage drop at a given J increases with increasing temperature. This behavior is called inversion. The voltage drop at the inversion point is about 1V, which is very close to that in Ref. [22]. Such an "inversion" is also observed in Si homojunction diodes and SiC diodes[23]. At higher temperature, 480K, it is found that the J-V curve does not obey the "inversion" behavior, the current density is much higher than that at low temperature. These phenomena relate to the temperature dependence of the resistivity of Si and will be discussed below in details.

Mnatssakanov *et al.*[23] used an equation to estimate the parameters of electron-hole scattering in silicon carbide. We find that the equation could be used to simulate and analysis the J-V data of the SiC/Si HJD's measured at the four different temperatures, but the ideality factor n should be included. Then the total voltage drop V across the structure at a given density J can be expressed as

$$V = \frac{nk_BT}{q}\ln\frac{J}{J_0} + A(T)\sqrt{J} + B(T)J \quad (1)$$

where k_B and T are Boltzmann's constant and the absolute temperature, respectively. J_0 is proportional to J_s, which is the saturation current density of the HJD's. The first term in equation (1) is the voltage drop across the 3C-SiC/Si heterojunction. The second is the ohmic voltage due to scattering on phonons, impurities, and dislocations. The third consists of the ohmic voltage drop associated with electron-hole scattering and the voltage due to total contact resistance and the series resistance.

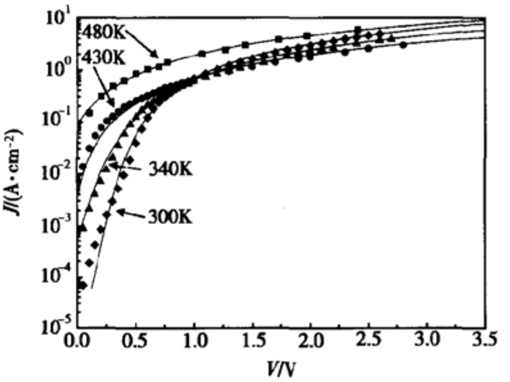

Fig. 3 Isothermal J-V characteristics of the SiC/Si HJD Points represent experimental data measured at different temperatures. Lines show J-V characteristics calculated for the same temperature.

Equation (1) makes it possible to determine the values of the parameters n, J_0, A, and B by means of fitting to the experimental J-V characteristics in a wide temperature region. Applying the least-squares method to achieve the best fit to the experimental data, we obtain the values for the parameters in Table 1.

Table 1 Best fit values of parameters to the experimental data

T/K	n	J_0/(A·cm^{-2})	A	B/(Ω·cm^2)
480	1	2.5	0.4	0.242
430	1	0.028	0.8	0.42
340	1.5	0.00038	0.6	0.28
300	1.8	0.00003	0.41	0.22

From the Arrhenius plot of J_0 in Fig. 4, the activation energy ΔE_{as} is obtained to be 0.749 eV, which is equal to qV_{bi}. Therefore, the activation energy ΔE_{as} is due to the built-in voltage of the HJ. This indicates that the forward current is dominated by the thermionic emission of carriers over a potential barrier of height V_{bi}. Diffusion mechanics can also draw the same conclusion that ΔE_{as} is the same as the built-in voltage of the HJ[24]. The ideality factor, n, is obtained to be 1.8 at 300K, suggesting that the generation-recombination processes could not be neglected. The value of n decreases because the diffusion current increases faster than the recombination current with the increasing temperature and at high temperature the diffusion current dominates[25].

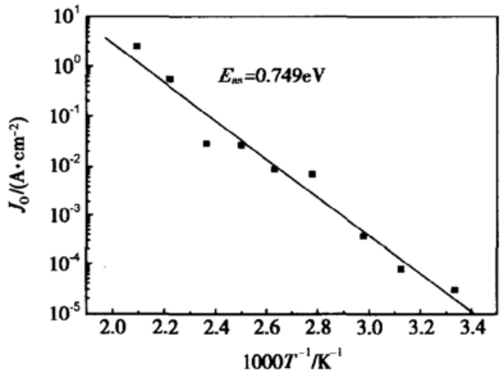

Fig. 4 Arrhenius plots of the value of the parameter J_0

The temperature dependence of the values of A and B in Table 1 is favorable in understanding the "inversion" behavior when $T<$ 430K and the rapid increase of the forward current when $T>$ 430K. When 300K$<T<$ 430K, all the dopants in Si have completely ionized, and therefore scattering on phonons and impurities dominat. Thus the resistivity increase with increasing temperature and the "inversion" behavior becomes easily understood. However, when $T>$ 430K, the carrier concentration due to intrinsic excitation exceeds $1\times10^{14}cm^{-3}$, which is about ten percent of the acceptor concentration of the p-type Si substrate we employ. Namely, the carrier concentration due to intrinsic excitation becomes comparable to the acceptor concentration of the substrate. Therefore, the intrinsic excitation rapidly dominates and the resistivity sharply decreases with further increasing temperature. As a result, the forward current rapidly increases with increasing temperature when $T >$ 430K.

3.3 Temperature dependence of forward and reverse current

Figure 5 shows the forward and reverse current density at bias voltage of ±1V. The reverse current density due to generation in the space-charge region increases rapidly with the increasing temperature, while the forward current density increases slowly with the increasing temperature up to 430K. When the temperature is higher than 430K, the forward current density increases rapidly. This result is consistent with that obtained in high temperature *I-V* data. And it is due to the intrinsic excitation of Si at higher temperature as discussed above.

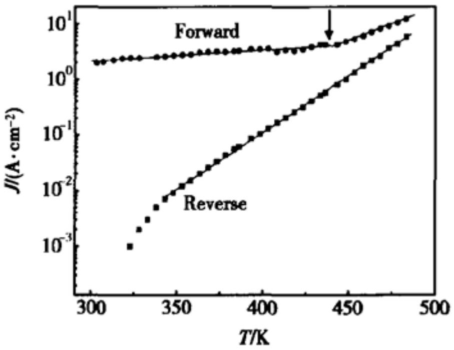

Fig. 5 Temperature dependence of the current density at ±1V bias for the SiC/Si HJD

4 Conclusion

The n-3C-SiC/p-Si HJD fabricated by low pressure chemical vapor deposition (LPCVD) showes good rectifying properties at room temperature. Capacitance-voltage characteristics show that the abrupt junction model is applicable to the SiC/Si HJ and the built-in voltage V_{bi} is 0.75V. The high temperature (300~480K) characteristics of the HJD are investigated. And an equation is presented to simulate and explain the forward *I-V* data measured at various temperatures. The conduction mechanisms are determined by analyzing the current-voltage characteristics. The 3C-SiC/Si HJD represents a promising approach for the fabrication of HJ devices such as SiC-emitter HBT.

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3C-SiC/Si 异质结二极管的高温特性*

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摘要: 研究了低压化学气相淀积方法制备的n-3C-SiC/p-Si(100)异质结二极管(HJD)在300~480K高温下的电流密度-电压(J-V)特性. 室温下HJD的正反向整流比(通常定义为±1V外加偏压下)最高可达1.8×10^4, 在480K时仍存在较小整流特性, 整流比减小至3.1. 在300K温度下反向击穿电压最高可达220V. 电容-电压特性表明该SiC/Si异质结为突变结, 内建电势V_{bi}为0.75V. 采用了一个含多个参数的方程式对不同温度下异质结二极管的正向J-V实验曲线进行了很好的拟和与说明, 并讨论了电流输运机制. 该异质结构可用于制备高质量异质结器件, 如宽带隙发射极SiC/Si HBT等.

关键词: LPCVD; 异质结二极管; 高温特性

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