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Degradation of pMOSFETs with Ultrathin Oxide and Different HALO Dose*

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Abstract: The effect of HALO dose on device parameter degradation of pMOSFET with 2.1nm oxide and 0.135μm channel length at hot carrier stress is analyzed. It is found that the degradation mechanism is not sensitive to HALO dose changing, but the degradation quantities of linear drain current, saturation drain current, and maximum transconductance increase with HALO dose enhancing and are larger than those of speculated before. The degradation of device parameters (linear drain current, saturation drain current, and maximum transconductance) is attributed to not only the drain series resistance enhancing induced by interface states under spacer oxide and carrier mobility degradation but also the threshold voltage variation and initial threshold voltage increasing with HALO dose enhancing.

Key words: hot carrier; pMOSFET; HALO; degradation
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1 Introduction

For short channel VLSI transistors, the drain to source punch through is a serious problem when device scaling goes on continuously. HALO structure is added to prevent punch through and to improve the threshold voltage roll-off characteristic[1,2]. Some results about HALO structure have been reported[3~5]. It is found that, larger tilt implant low energy HALO devices show less degradation at hot carrier stress. However, when device characteristic dimension comes into sub-0.15μm and the gate oxide is ultra thin, though drain current model and hot carrier degradation of HALO structure devices have been published[6,7], the effect of HALO dose on device degradation at hot carrier stress has not been reported and the analytical model of drain current degradation at hot carrier stress due to HALO dose changing has not been studied carefully.

In this paper, the effect of HALO dose on pMOSFET device performance (I_{dsat}, I_{dline}, g_m, and V_{th}) degradation under hot carrier stress is investigated. At first, the experimental set in this work is described. In the second part, the experimental results are shown to study the correlation between degradation mechanism and HALO doses after hot carrier stress. Finally, then the difference of parameter degradation quantities due to the HALO dose

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changing is discussed and modeled.

2 Experiment

All measured devices are pMOSFETs with 10μm channel width (W) and 0.135μm channel length (L). The gate oxide thickness is about 2.1nm measured by C-V and simulation method. The test devices are divided into three groups by the HALO dose. Group Ⅰ named P1, its HALO dose is minimum, group Ⅱ named P2 and group Ⅲ named P3, their HALO doses are respectively two and four times of the group Ⅰ. Other technology conditions are similar to Ref. [5].

HP4156B semiconductor parameter analyzer and HP16440A pulse generator were used to perform the hot carrier stress, to monitor device performance degradation, and to measure charge pumping current. The stress drain bias is from -2.6V to -3.0V at room temperature. The linear drain current is extracted by biasing at $V_g=-1.5$V, $V_d=-0.1$V; the saturation drain current is extracted by biasing at $V_g=V_d=-1.5$V; the threshold voltage is extracted by the defined drain current $W/L\times10^{-7}$A, and the maximum transconductance is extracted by the maximum differential value of the transfer characteristic curves in linear region. The saturation drain current degradation $\mathrm{d}I_{dsat}(\Delta I_{dline}/I_{dsat0})$, the linear drain current degradation $\mathrm{d}I_{dline}(\Delta I_{dline}/I_{dline0})$, the threshold voltage variation $\Delta V_{th}(V_{th}-V_{th0})$, and the maximum transconductance degradation $\mathrm{d}g_m(\Delta g_m/g_{m0})$ are examined to characterize the device performance degradation at hot carrier stress.

3 Results and discussion

Figure 1 shows the I_{dsat} degradation of P3 under $V_g=V_d$ and $V_g=V_d/2$ stress modes, the drain bias is from -2.6V to -3.0V. In this plot, at the same stress mode, the higher the stress voltage, the higher the saturation drain current degradation, also, the degradation lines are parallel to each other.

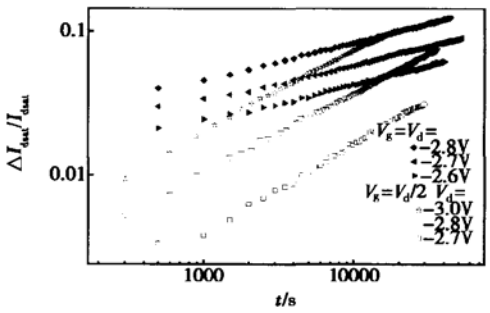

Fig. 1 I_{dsat} degradation of devices with HALO dose P3 under $V_g=V_d$ and $V_g=V_d/2$ stress modes

It can be seen that all characteristic lines follow the well-known power law[8]. The relationship can be written as

$$\Delta = At^n \tag{1}$$

where Δ is the parameter degradation quantity, t is stress time, n is the degradation time factor which is sensitive to degradation mechanism and technology. It can also be seen that all degradation lines at each stress mode fit well, the degradation time factor, n, under $V_g=V_d$ stress mode is about 0.3 by linear fit, but n is about 0.6 under the $V_g=V_d/2$ stress mode. It indicates that $V_g=V_d/2$ stress mode is the worst-case stress mode after long time accelerated stress, so following studies would focus on $V_g=V_d/2$ stress mode.

The saturation drain current degradation of P1, P2, and P3 stressed under $V_g=V_d/2=-1.4$V is shown in Fig. 2(a). The three degradation lines are parallel and the degradation quantity increases as HALO dose increases. For other biased drain voltages from -3.0V to -2.6V, the experimental results are similar. Using other parameters characterizing the devices degradation, such as the degradation of maximum transconductance in Fig. 2(b) and threshold voltage variation in Fig. 2(c), the same degradation law can be found. Thus, it can be concluded that the degradation mechanism is not sensitive to the changing of HALO dose, while the parameter degradation quantities are sensitive to the changing of HALO dose.

In Fig. 3, the $\mathrm{d}I_{dline}$, $\mathrm{d}I_{dsat}$, $\mathrm{d}g_m$, and ΔV_{th} versus

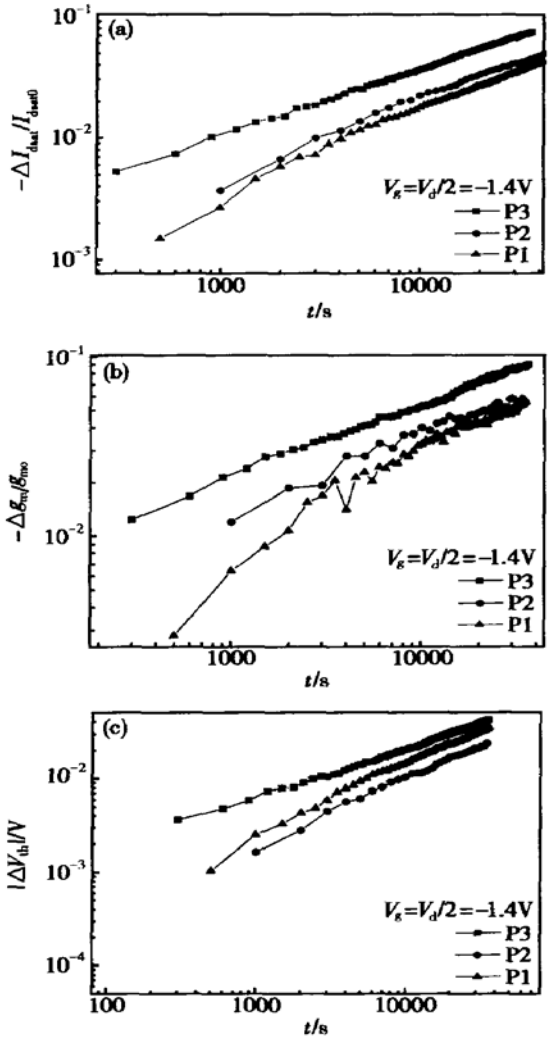

Fig. 2 I_{dsat} degradation (a), g_m degradation (b), threshold voltage variation (c) of devices with HALO dose P1, P2, and P3 under $V_g = V_d/2$ stress mode

normalized HALO dose stressed at $V_g = V_d/2 = -1.4$V stress mode after 12000s is plotted.

I_{dsat}, I_{dline}, and g_m degradation increase with the HALO dose increasing, which are different from using 0.2μm technology with extension HALO implants and a physical oxide thickness of 3.5nm reported in Ref. [5]. But the threshold voltage variations are less than 10mV. The parameter degradations at other stress voltages from −3.0V to −2.6V are similar. So, the following study of HALO dose effect will focus on the degradation of dI_{dline}, dI_{dsat}, and dg_m.

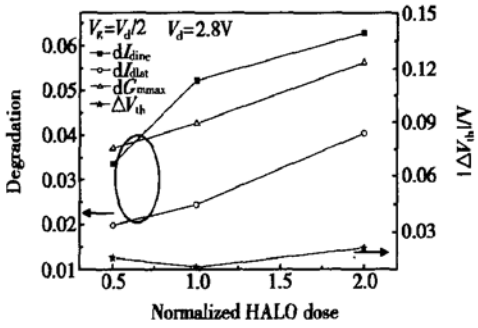

Fig. 3 dI_{dline}, dI_{dsat}, and dg_m and ΔV_{th} versus normalized HALO dose stressed at $V_g = V_d/2 = -1.4$V after 12000s

To investigate the experimental results, the correlation between HALO doses and channel electric field should be studied first. As we know, with enhanced HALO dose, the threshold voltage will be higher. By three-transistor threshold voltage model[9], the threshold voltage can be expressed by:

$$V_{th} = V_{tc} + \frac{kT}{q}\ln\left[1 + \frac{2L_h}{L}\left(e^{\frac{q}{kT}(V_{tHALO} - V_{tc})} - 1\right)\right] \quad (2)$$

$$V_{tHALO} = V_{fb} + 2\Phi_f + \gamma\sqrt{2\Phi_f + V_{sb}} = V_{FB} + 2\frac{kT}{q}\ln\frac{N_b}{N_i} + \gamma\sqrt{2\frac{kT}{q}\ln\frac{N_b}{N_i} + V_{sb}} \quad (3)$$

where V_{tc} is the channel region threshold voltage, V_{tHALO} is the HALO region threshold voltage; L_h is the HALO region length; N_b is the HALO region substrate concentration. For different HALO doses, V_{tc} is constant, but V_{tHALO} increases when HALO dose becomes larger.

So the saturation drain voltage V_{dsat}, which can be expressed by[10]

$$V_{dsat} = \frac{|V_g - V_{th}|_{eff}E_c}{|V_g - V_{th}| + L_{eff}E_c} = \frac{1}{\frac{1}{L_{eff}E_c} + \frac{1}{\left|V_g - V_{tc} - \frac{kT}{q}\ln\left[1 + \frac{2L_h}{L}\left(e^{\frac{q}{kT}(V_{tHALO} - V_{tc})} - 1\right)\right]\right|}} \quad (4)$$

Then, the maximum lateral electric field is:

$$E_m \approx \frac{V_d - V_{dsat}}{l} \quad (5)$$

it will become larger with the increasing of HALO dose.

The substrate current is decided by the maxi-

mum electric field[11].

$$\frac{I_b}{I_d} = ce^{-\frac{Bi}{E_m}} \tag{6}$$

When the HALO dose increases, the maximum electric field augments, the I_b/I_d will strengthen at the same bias with HALO dose increasing. The experimental results are shown in Fig. 4(a) and the bigger $|V_d|$, the larger I_b/I_d. Figure 4(b) is the calculated lateral electric field versus HALO doses, which directly proves that the maximum lateral electric field, E_m, increases with the HALO dose increasing which leads to the increasing of degradation.

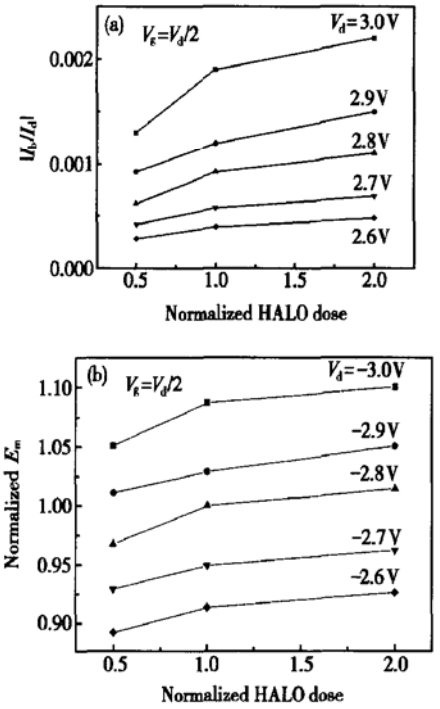

Fig. 4 $|I_b/I_d|$ versus normalized HALO dose (a) and the calculated maximum electric field versus normalized HALO dose (b) when biased on $V_g = V_d/2$ mode

Additionally, the impact ionization mainly generated at the peak spot of electric field, because the maximum electric field locates in the LDD region, the interface states and charges trapping will be mainly produced there. Generally speaking, when the gate oxide thickness is below 4.5nm, the oxide trapping is negligible[12]. In this paper, the gate oxide thickness of all test devices is 2.1nm, so all device degradations are mainly influenced by interface states[13].

Figure 5 shows the correlation between stress time and charge pumping current variation of P1, P2, and P3. The tested devices were biased at $V_g = V_d/2$ mode and the drain bias is − 2.8V.

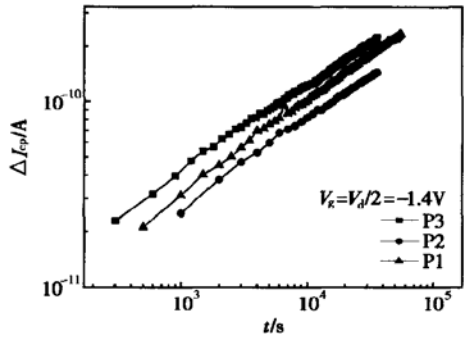

Fig. 5 Charge-pumping current variation versus the stress time when stress at $V_g = V_d/2$ stress mode The drain bias is − 2.8V.

Figure 5 shows that ΔI_{cp} of P3 is the biggest, ΔI_{cp} of P2 is the smallest. That is to say, the enhancing lateral maximum electric field does not necessarily lead to generate more interface states with HALO dose increasing.

The generated interface state density can be described by[11]

$$N_{it}(t) = C\left(t\frac{I_{ds}}{W}e^{-\frac{Bi}{E_m}}\right)^m \tag{6}$$

where C is a fitting constant, t is stress time, and m is a simulation parameter. m is about 0.48 in our experiments. The generated interface state density is a function of both impact ionization rate and drain current. From the above discussion, the maximum lateral electric field increases with increased HALO dose, but the drain current will decrease for the enhanced threshold voltage. Thus, the lateral maximum electric field enhancing does not necessarily lead to more interface states with increased HALO dose, just like what are described in Ref. [5] that the increased HALO doping concentration

does not necessarily lead to more defect generations.

In Fig. 6, at the same linear drain current degradation, such as 3% or 4%, the charge pumping current variation decreases with HALO dose increasing, and at the same charge pumping current variation, the linear drain current degradation increases and trends to saturate with HALO dose increasing.

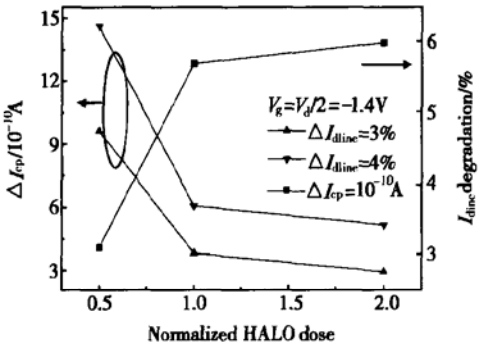

Fig. 6 Relationship between ΔI_{cp}, $-\Delta I/I_{dline0}$, and normalized HALO dose

According to the well known two-stage degradation model[14], the generated interface states are distributed over channel region and under spacer oxide region. The interface states under spacer oxide region increase the drain series resistance; the interface states near the drain edge decrease the carrier mobility.

As we know, I_{dline} can be described as[15]

$$I_{dline} = \mu_0 C_{ox} \frac{W}{L}(V_g - V_{th0} - 0.5V_d)V_d \quad (7)$$

But, after hot carrier stress, I_{dline} should be written as

$$I_{dline}' = \frac{\mu_0}{1+\beta N_{it}} C_{ox} \frac{W}{L}[V_g - (V_{th0} + \Delta V_{th}) - 0.5V_d']V_d' \quad (8)$$

where $V_d' = V_d - I_d\Delta R_d$ is the effective drain voltage dropped into the source and channel region, ΔR_d is the increased drain series resistance caused by interface states under the spacer silicon oxide, it decreases the effective drain voltage. Here threshold voltage and the carrier mobility becomes $V_{th0}+\Delta V_{th}$ and $\frac{\mu_0}{1+\beta N_{it}}$ respectively because of generated interface states, where β is a fitting constant and varies with different HALO doses.

Then the linear drain current degradation can be described as

$$\Delta I_{dline}/I_{dline0} = \frac{V_d - I_d\Delta R_d}{1+\beta N_{it}}\left[\frac{1}{V_d} + \frac{0.5I_d\Delta R_d}{(V_g - V_{th0} - 0.5V_d)V_d} - \frac{\Delta V_{th}}{(V_g - V_{th0} - 0.5V_d)V_d}\right] - 1 \quad (9)$$

From equation (9), the linear drain current degradation is a function of drain series resistance ΔR_d, threshold voltage V_{th0}, and threshold voltage variation ΔV_{th}. ΔR_d trends to saturate after long time stress and increases with HALO dose increasing. In our experiments ΔR_d is less than 20Ω extracted by S&R method[15] and the maximum difference of ΔR_d between P1, P2, and P3 is about 14Ω. The linear drain current, I_d, which are about 0.45, 0.5, and 0.65mA for P3, P2, and P1, respectively. The threshold voltages of P3, P2, and P1 before hot carrier stresses are about −0.4, −0.3, and −0.1V, respectively. The threshold voltage variations ΔV_{th} of devices with different HALO doses are about 20mV. Thus with the threshold voltages increasing, the linear drain current degradation increases. In other words, the increasing threshold voltage mainly affects the linear drain current degradation as HALO dose increases. Because the threshold voltage of P2 and P3 are close and larger than that of P1, the linear drain current degradations increase with HALO dose increasing and trend to saturate. With suitable fitting parameter β, the calculated linear drain current degradations by equation (9) are consistent to experimental results.

Similarly, the I_{dsat} can be expressed as[15]

$$I_{dsat} = \mu_0 \frac{W}{L} C_{ox}(V_g - V_{th0})^2(1 + \lambda V_d)$$

After hot carrier stress, I_{dsat} should be written as

$$I_{dsat}' = \frac{\mu_0}{1+\beta N_{it}} \times \frac{W}{L} C_{ox}[V_g - (V_{th0} + \Delta V_{th})]^2 \times$$

$$[1+\lambda(V_d-I_d\Delta R_d)]$$

Then

$$\Delta I_{dsat}/I_{dsat0}=\frac{1}{1+\beta N_{it}}\left(\frac{V_g-V_{th0}-\Delta V_{th}}{V_g-V_{th0}}\right)^2\times\left(1-\frac{\lambda I_d\Delta R_d}{1+\lambda V_d}\right)-1 \quad (10)$$

Also, g_m can be expressed as[15]

$$g_m=2\mu_0\frac{W}{L}C_{ox}(V_g-V_{th0})(1+\lambda V_d)$$

After hot carrier stress,

$$g_m'=\frac{2\mu_0}{1+BN_{it}}\times\frac{W}{L}C_{ox}[V_g-(V_{th0}+\Delta V_{th})]\times[1+\lambda(V_d-I_d\Delta R_d)]$$

So, g_m degradation should be

$$\Delta g_m/g_{m0}=\frac{1}{1+\beta N_{it}}\left(\frac{V_g-V_{th0}-\Delta V_{th}}{V_g-V_{th0}}\right)\times\left(1-\frac{\lambda I_d\Delta R_d}{1+\lambda V_d}\right)-1 \quad (11)$$

here λ is the channel length modulation factor.

From equations (10) and (11), the saturation drain current degradation and the maximum transconductance degradation are also associated with the drain series resistance, threshold voltage and threshold voltage variation. Because λ is about 0.1V and I_d is about 10^{-3}A, thus $\lambda I_d\Delta R_d \ll 1+\lambda V_d$, and the effect of $\frac{\lambda I_d\Delta R_d}{1+\lambda V_d}$ is negligible, so the I_{dsat} and g_m degradation are also mainly determined by threshold voltage and threshold voltage variation.

4 Conclusion

In this paper, the effect of HALO dose on device degradation of pMOSFET with 2.1nm ultra-thin gate oxide and 0.135 μm channel length under $V_g=V_d/2$ stress mode is investigated. As the HALO dose increases, the drain current decreases and the threshold voltage increases. After HCI stress, the device degradation mechanism is not sensitive to HALO dose changing, but the device parameter degradation worsens with HALO doses increasing and the difference of parameter degradation quantity is larger than that of speculated in published reference[5]. The analytical expressions of the device parameter (dI_{dline}, dI_{dsat}, dg_m) degradation are modeled and discussed. The parameter degradations (dI_{dline}, dI_{dsat}, dg_m) are attributed to drain series resistance increasing and carrier mobility reduction caused by interface states. The quantities of device parameter degradation are determined by the evolution of drain series resistance, threshold voltage, and threshold voltage variation. Though the generated interface states do not necessarily increase with HALO dose increasing, the initial threshold voltage plays an important role in the degradation and determines the parameter degradation finally. So, when the HALO structure is used to reduce the device short channel effect and restrain punch-through, the lower HALO dose should be chosen to decrease the device parameter degradations.

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不同 HALO 掺杂剂量的超薄栅 pMOSFET 的退化*

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摘要: 研究了热载流子应力下栅厚为 2.1nm，栅长为 0.135μm 的 pMOSFET 中 HALO 掺杂剂量与器件的退化机制和参数退化的关系. 实验发现，器件的退化机制对 HALO 掺杂剂量的改变不敏感，但是器件的线性漏电流、饱和漏电流、最大跨导的退化随着 HALO 掺杂剂量的增加而增加. 实验同时发现，器件参数的退化不仅与载流子迁移率的退化、漏串联电阻增大有关，而且与阈值电压的退化和应力前阈值电压有关.

关键词: 热载流子；pMOS 器件；HALO 结构；退化

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