第 25 卷第 10 期 半 导 体 学 报 Vol. 25, No. 10
2004 年 10 月 CHINESE JOURNAL OF SEMICONDUCTORS Oct., 2004

HfO_2 Gate Dielectrics for Future Generation of CMOS Device Application

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Abstract: The material and electrical properties of HfO_2 high-k gate dielectric are reported. In the first part, the band alignment of HfO_2 and $(HfO_2)_x(Al_2O_3)_{1-x}$ to (100) Si substrate and their thermal stability are studied by X-ray photoelectron spectroscopy and TEM. The energy gap of $(HfO_2)_x(Al_2O_3)_{1-x}$, the valence band offset, and the conduction band offset between $(HfO_2)_x(Al_2O_3)_{1-x}$ and the Si substrate as functions of x are obtained based on the XPS results. Our XPS results also demonstrate that both the thermal stability and the resistance to oxygen diffusion of HfO_2 are improved by adding Al to form Hf aluminates. In the second part, a thermally stable and high quality HfN/HfO_2 gate stack is reported. Negligible changes in equivalent oxide thickness (EOT), gate leakage, and work function (close to Si mid-gap) of HfN/HfO_2 gate stack are demonstrated even after 1000℃ post-metal annealing (PMA), which is attributed to the superior oxygen diffusion barrier of HfN as well as the thermal stability of the HfN/HfO_2 interface. Therefore, even without surface nitridation prior to HfO_2 deposition, the EOT of HfN/HfO_2 gate stack has been successfully scaled down to less than 1nm after 1000℃ PMA with excellent leakage and long-term reliability. The last part demonstrates a novel replacement gate process employing a HfN dummy gate and sub-1nm EOT HfO_2 gate dielectric. The excellent thermal stability of the HfN/HfO_2 gate stack enables its use in high temperature CMOS processes. The replacement of HfN with other metal gate materials with work functions adequate for n- and p-MOS is facilitated by a high etch selectivity of HfN with respect to HfO_2, without any degradation to the EOT, gate leakage, or TDDB characteristics of HfO_2.

Key words: high-k gate dielectrics; HfO_2; hafnium aluminates; HfN; metal gate electrode
EEACC: 2810; 2570D
CLC number: TN386 **Document code**: A **Article ID**: 0253-4177(2004)10-1193-12

1 Introduction

High-k gate dielectrics have been extensively studied as alternates to conventional gate oxide (SiO_2) due to the aggressive downscaling of SiO_2 thickness in CMOS devices, and hence the excessive gate leakage. HfO_2 has emerged as one of the most promising high-k candidates due to its high dielectric constant and compatibility with poly-silicon deposition process[1,2]. However, it suffers recrystallization during high temperature post process annealing, which would induce high leakage current and severe dopants penetration issues. Al has been proposed to alloy HfO_2 to raise its crystallization temperature[3]. In the first part of this paper, we report the energy gap (E_g) of $(HfO_2)_x(Al_2O_3)_{1-x}$, the valence band offset (ΔE_v) and the conduction band offset (ΔE_c) between $(HfO_2)_x(Al_2O_3)_{1-x}$ and the Si substrate as functions of x

Received 17 June 2004

obtained based on X-ray photoelectron spectroscopy (XPS) measurement. Furthermore, the thermal stability of Hf aluminates and its impact on oxygen diffusivity through Hf aluminates are studied.

Another major concern regarding the application of HfO_2 gate dielectric is the fact that HfO_2 is a poor barrier to oxygen diffusion, which would cause the uncontrolled growth of low-k interfacial layer (IL) between HfO_2 and Si substrate during high-temperature post-processing and hence impose serious concern to equivalent oxide thickness (EOT) scalability[1,4]. Although using surface nitridation (SN) or N-contained HfO_2 (i.e. HfO_xN_y) can minimize IL growth[5,6], they also cause severe carrier mobility degradation. In the second part of this paper, we present the thermally robust high quality gate stack composing of HfN metal gate/HfO_2 gate dielectric with excellent EOT scalability against high temperature treatments, without using SN prior to HfO_2 deposition, and investigate its performance and reliability for MOS device applications. The application of metal gate electrodes would address the concerns associated with conventional poly-Si gate electrodes, such as the poly-Si gate depletion, dopant penetration, and high gate sheet resistance in the aggressively scaled CMOS transistors.

Two metal gate electrodes with different work functions are required to achieve optimal device performance in n- and p-channel transistors[7]. Immense process challenges are faced in the integration of dual-metal gates in CMOS transistors with sub-1nm EOT high-k dielectric, such as HfO_2[8,9]. Issues such as interfacial reaction of the metal gate with the underlying gate dielectric and the variation of metal gate work function Φ_m with annealing temperature may limit the use of high thermal budget process steps after metal gate formation[8]. A replacement gate process that forms the metal gate electrode after the activation of the source/drain (S/D) dopants is therefore attractive[10,11]. In a conventional replacement gate process, high-k dielectric and metal-gate electrode replaces the poly-Si dummy gate and underlying sacrificial SiO_2 after S/D dopant activation anneal. Nevertheless, high-temperature anneal of high-k dielectric is required for better carrier mobility, less fixed charge and less C-V hysteresis[11,12]. High-temperature post-deposition anneal (PDA) of high-k dielectric before metal gate deposition, however, will cause a EOT increase which is a serious concern for aggressive CMOS scaling. In the last part of this paper, a novel replacement gate process employing a dummy HfN gate electrode material is demonstrated to integrate dual-metal gate electrodes with sub-1nm HfO_2 gate dielectric. The HfN/HfO_2 gate stack shows excellent thermal stability during the source/drain dopant activation, allowing sub-1nm EOT and good dielectric characteristics to be achieved[13]. In addition, the high etch selectivity of HfN with respect to HfO_2 enables it use as a dummy gate electrode in a replacement gate process without degrading the HfO_2 dielectric. This makes HfN more attractive than poly-Si dummy gate. Replacement of the dummy HfN gate with Ta for NMOS and Ni for PMOS devices is also demonstrated. The work function difference between NMOS and PMOS gate electrodes is about 0.8eV.

2 Material characterizations of HfO_2 and $(HfO_2)_x(Al_2O_3)_{1-x}$ by XPS and TEM

$(HfO_2)_x(Al_2O_3)_{1-x}$ ($0 \leqslant x \leqslant 1$) films of five various compositions were prepared by atomic layer deposition (ALD) at 300℃ wafer temperature, with 200mm. p-type (100) Si wafers as substrates. To evaluate the thermal stability of the Hf aluminates, rapid thermal annealing (RTA) was conducted in 1.3×10^3Pa of N_2 or in high vacuum (~ 2.7×10^{-3} Pa) at several temperatures (800~1000℃) for 20s. The ex-situ high resolution XPS were taken to measure the Al 2p, Hf 4f, C 1s, O 1s, valence band maximum (VBM), and O 1s energy loss spectra. All of the high-resolution scans were

taken at a photoelectron take-off angle of 90° and with a pass energy of 20eV. The intensities for all the XPS spectra reported here have been normalized for comparison and all of the spectra are calibrated against C 1s peak (285.0eV) of adventitious carbon. The XPS results show that all Hf aluminates samples possess nice stoichiometry, and their compositions could be expressed as HfO_2, $(HfO_2)_{0.85}$-$(Al_2O_3)_{0.15}$, $(HfO_2)_{0.67}$ $(Al_2O_3)_{0.33}$, $(HfO_2)_{0.41}$-$(Al_2O_3)_{0.59}$, and Al_2O_3 respectively.

Figure 1(a) depicts O 1s energy losses spectra for various as-deposited $(HfO_2)_x(Al_2O_3)_{1-x}$ samples, which is caused by the outgoing photoelectrons suffering inelastic losses to collective oscillations (plasmon) and single particle excitations (band to band transition)[14]. The energy band gap values (E_g) could be determined by the onset of energy loss from their respective spectrum. By this means, the energy gap for HfO_2 is measured as 5.25 ± 0.1eV and for Al_2O_3 as 6.52 ± 0.1eV. The energy gap value of Al_2O_3 is consistent with reported by other research groups[15]. It is worthy noting the continuous change in the energy loss spectra contour occurs with Hf(Al) composition variation.

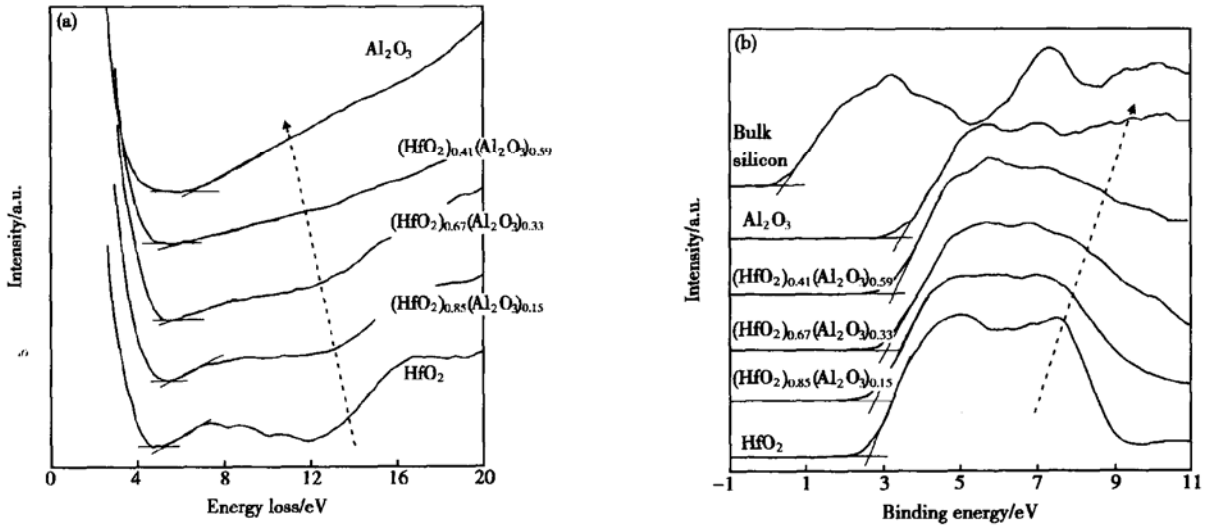


Fig. 1 (a) O 1s energy losses spectra for various $(HfO_2)_x(Al_2O_3)_{1-x}$ samples. The cross point denotes the band gap (E_g) value for each sample. Dashed arrow shows the constantly change in the energy loss spectra contour with Hf aluminates composition. (b) XPS valence band spectra taken from various $(HfO_2)_x(Al_2O_3)_{1-x}$ samples and H-terminated bulk Si. The cross point from each spectrum denotes the valence band maximum (VBM) for that specific sample. The valence band alignment is yielded by the difference of VBM between the $(HfO_2)_x(Al_2O_3)_{1-x}$ and the H-terminated Si. The dashed arrow indicates the gradual change in the valence band density of states Hf aluminates composition.

The determination of valence band alignment of $(HfO_2)_x(Al_2O_3)_{1-x}$ on Si substrate is performed by measuring the difference of VBM between the $(HfO_2)_x(Al_2O_3)_{1-x}$ samples and the hydrogen-terminated Si(100) substrate, as shown in Fig. 1(b). The VBM for each sample is defined by extrapolating the leading edge of VB to the baseline (the cross point). Therefore, ΔE_v values of 3.03 ± 0.05eV and 2.22 ± 0.05eV could be obtained for Al_2O_3 and HfO_2, respectively. We again observe the gradual changes in the valence band density of states with Hf(Al) composition variation.

With the knowledge of Si energy gap value (1.12eV), the conduction band offset for $(HfO_2)_x$-$(Al_2O_3)_{1-x}$ can be simply derived by the equation of

$$\Delta E_c = E_g - \Delta E_v - 1.12(\text{eV})$$

where ΔE_c for HfO_2 is calculated as 1.91 ± 0.15eV and for Al_2O_3 as 2.37 ± 0.15eV. The relationship

between E_g, ΔE_v, and ΔE_c values for $(HfO_2)_x(Al_2O_3)_{1-x}$ and the Hf composition is summarized in Fig. 2. Linear dependence on composition is revealed for E_g, ΔE_v, and ΔE_c based on XPS measurement.

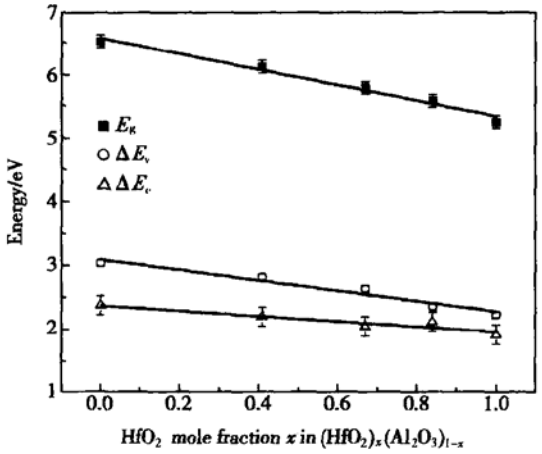


Fig. 2 Dependence of E_g, ΔE_v, and ΔE_c of $(HfO_2)_x(Al_2O_3)_{1-x}$ on Hf composition

Next, we discuss the thermal stability of the Hf aluminates. High-resolution XPS was applied to quantitatively study the growth of the IL between $(HfO_2)_x(Al_2O_3)_{1-x}$ films and Si substrate during RTA processing. The Si 2p core level XPS spectra for these $(HfO_2)_x(Al_2O_3)_{1-x}$ samples of as-deposited and after various RTA processes (800℃/N_2, 900℃/N_2, 1000℃/N_2, and 1000℃/high vacuum) are shown as Fig. 3. The peak located at 99.3eV is assigned to Si- Si bonds from Si substrates, and the other one at 103.0eV to Hf(Al) silicate bonds from the IL. It is seen that an IL exists for all of the as-deposited samples. The change in the peak intensity of IL silicate directly correlates with the growth of the IL: the higher the intensity, the thicker the IL. For a given annealing temperature, the extent of IL growth is determined versus Al%, with HfO_2 film (0% Al) showing the largest growth, and Al_2O_3 film the smallest. Doping of HfO_2 film with Al slows down the IL growth during annealing. Based on these XPS results, one can draw the conclusion that the ability to block oxygen diffusion through HfO_2 films is greatly en-

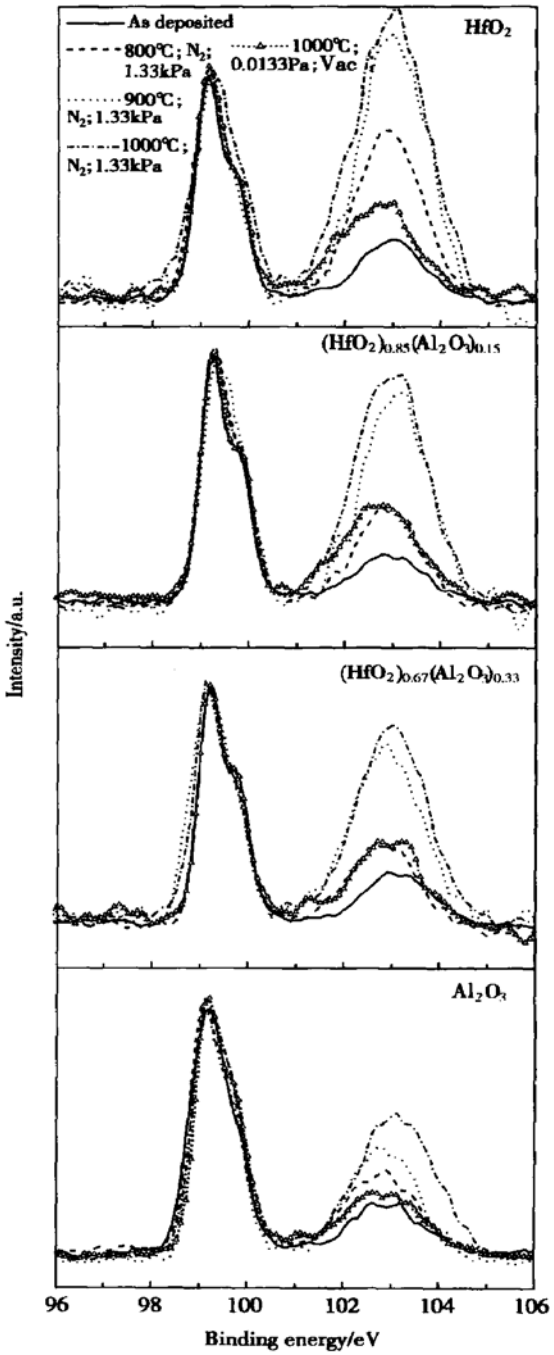


Fig. 3 XPS Si 2p core level spectra recorded from various $(HfO_2)_x(Al_2O_3)_{1-x}$ samples (the thin ones) of as-deposited (solid lines), after 800℃/N_2 annealing (dashed lines), 900℃/N_2 annealing (dotted lines), 1000℃/N_2 annealing (dashed dotted lines), and 1000℃/high vacuum annealing (dashed lines with open triangles) The peak located at ~ 99.3eV is assigned to Si- Si bonds from the substrates, and the one at ~ 103.0eV to Si- O bonds from IL. The intensities for XPS peaks of Si- Si bonds have been normalized for comparison.

hanced by the incorporating of Al, and the ability becomes stronger when more Al is incorporated. The Si 2p spectra for each sample annealed in high vacuum ($\sim 2.7\times10^{-3}$ Pa) at 1000℃ is also shown in Fig. 3. The IL growth is significantly smaller than those of annealing in N_2 at the same temperature. This result implies that the active source of oxygen in N_2 ambient, not the oxygen species present in the high-k films themselves, is responsible for the IL growth during RTA.

The high-resolution cross-sectional transmission electron microscope (HRTEM) of two samples [HfO_2 and $(HfO_2)_{0.85}(Al_2O_3)_{0.15}$ films] before and after 900℃ annealing in N_2 are presented in Fig. 4. After annealing, it is observed that the growth of IL is greater for the HfO_2 sample compared to the Al doped HfO_2, consistent with the XPS results shown in Fig. 1. The composition of the IL is likely to be Hf(Al) silicate (with SiO_2 rich), which is supported by XPS measurements shown in Fig. 3. Another evidence for silicate formation is the high-k film thickness decrease after annealing, as shown by HRTEM images, which may be due to the consumption of high-k films through the reaction with IL and/or film densification.

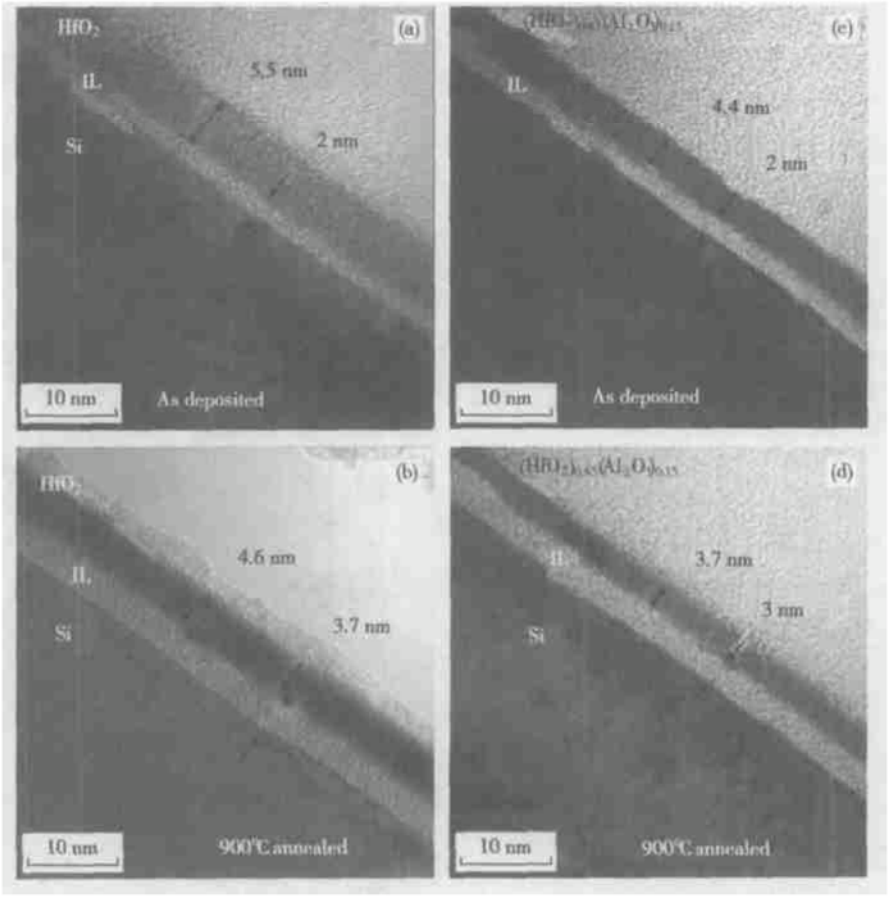


Fig. 4　HRTEM images for the as-is HfO_2 sample(a), the 900℃/N_2 annealed HfO_2 sample(b), the as-is $(HfO_2)_{0.85}(Al_2O_3)_{0.15}$ sample(c), and the 900℃/N_2 annealed $(HfO_2)_{0.85}(Al_2O_3)_{0.15}$ sample(d)

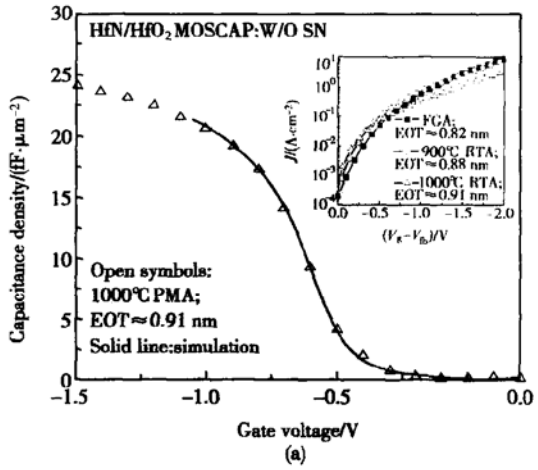
As pointed out previously, HfO_2 film crystallization temperature is increased through the alloy of Al. In addition, Hf aluminates films crystallization temperature increases when more Al is incorporated[3]. These facts are well correlated with the experimental observation in our study: the higher Al concentration, the higher the crystallization temperature, and hence the lower the oxygen diffu-

sion along the grain boundaries. Another reason for the reduced rate of oxygen diffusion by the addition of Al_2O_3 is that Al_2O_3 is known to have much lower oxygen diffusion coefficient compared to HfO_2 at high temperature[16].

3 Robust high-quality HfN/HfO_2 gate stack for advanced MOS device applications

In this part, both MOS capacitors (MOSCAPs) and MOSFETs devices with HfN/HfO_2 gate stack have been fabricated. The MOSCAPs were fabricated using p-Si(100) substrates. After the definition of the active area with 400nm field oxides and standard DHF-last RCA pre-gate clean, CVD HfO_2 films were deposited at 400℃ using $Hf[OC(CH_3)_3]_4$ and O_2 in a metal-organic chemical vapor deposition (MOCVD) cluster tool, followed by an in-situ PDA at 700℃ in N_2 ambient to improve film quality. 50nm HfN capped with 100nm TaN metal stacked layers were then deposited by DC sputtering of Hf/Ta target in Ar + N_2 mixed gas ambient, and patterned using a Cl_2-based RIE. The MOSCAPs were then rapid thermal annealed in N_2 at 900~ 1000℃ for 20s for thermal stability evaluation. For n-channel MOSFETs fabrication, source/drain implantation of phosphorus with a dose of $5\times10^{15}cm^{-2}$ was performed followed by RTA activation in N_2 at 950℃ for 30s. All devices were finally subjected to back side Al metallization and the forming-gas annealing (FGA) at 420℃ for 30min. EOT and flat band voltage (V_{fb}) were simulated by taking into account the quantum mechanical correction.

Figure 5(a) shows measured C-V curve(the symbols) of a HfN/HfO_2 device after 1000℃ post metal annealing(PMA), which is in good agreement with the simulation (the solid line). Without SN treatment, the EOT of the HfN/HfO_2 MOSCAP is as low as 0.82nm after FGA, and it slightly increases to 0.88nm/0.91nm after 900℃/1000℃ PMA. Negligible variation of the gate leakage current is observed in these devices after various thermal treatments, as shown in the inset of Fig. 5(a). HRTEM is utilized to characterize these HfN/HfO_2 gate stacks after various RTA, as shown in Fig. 5(b). Negligible change due to RTA in the physical thickness of both HfO_2 and IL is seen, consistent with results in Fig. 5(a). From the HRTEM and C-V data, it appears that the IL is not the pure SiO_2[1], and it has a k value of 7~ 8. Note



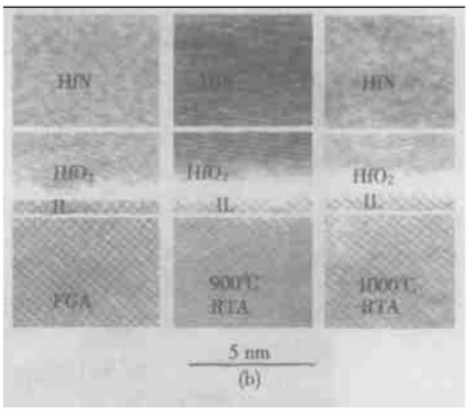


Fig. 5 (a) Comparison between C-V measurement data (symbols) and simulation data (the solid line) for HfN/HfO_2 n-MOSCAP after 1000℃ PMA annealing (with EOT ≈ 0.91nm) No surface nitridation was performed before HfO_2 deposition. The inset shows leakage comparison measured from the HfN/HfO_2 MOSCAP after various PMA process. (b) Cross-sectional HRTEM images of these HfN/HfO_2 MOSCAPs after different thermal treatments For FGA sample, IL is ~ 0.7nm and HfO_2 is ~ 2.2nm.

that at a gate voltage of V_{fb} - 1V, HfN/HfO_2 gate

stack demonstrates more than a factor of 10^5 reduction in the gate leakage as compared to poly Si/SiO_2 benchmark[17] at the same EOT (as shown in Fig. 6).

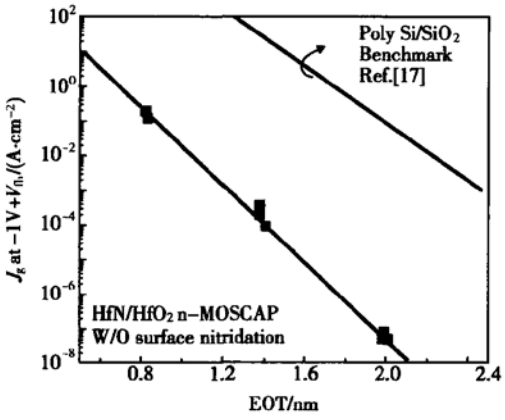


Fig. 6　Leakage versus EOT relationship for MOSCAP devices with HfN/HfO_2 gate stack

The work function (Φ_M) of HfN on HfO_2 is extracted from plots of V_{fb} versus EOT. Φ_M of HfN after FGA is 4.75eV and slightly increases to 4.8eV after 1000℃ PMA, and this small variation after 1000℃ RTA might be related to the HfN crystallization change and/or the Fermi pinning of the metal gate work function[22]. Nevertheless, these results suggest that the HfN/HfO_2 interface is thermally stable.

We also investigate the reliability of 1000℃ annealed HfN/HfO_2 gate stack. The typical stress-induced leakage current (SILC) time evolutions at four gate voltages (ranging from − 2.8V to − 3.4V) of the 1000℃ RTA treated HfN/HfO_2 device (EOT = 0.91nm) are shown in the inset of Fig. 7. Setting $\Delta J_g/J_{g_0}$ = 50% as failure criterion, the operating voltage for 10years lifetime is projected as 2.2V, as shown in Fig. 7.

Inset of Fig. 8(a) shows HFCV from a n-MOSFET (without SN treatment) with HfN/HfO_2 stack (EOT = 1.18nm from the *C*-*V*). The poly-depletion effect is suppressed as expected. Figures 8 (a) and (b) show the well-behaved electrical characteristics (I_d-V_g and I_d-V_d) of the n-MOSFET with excellent subthreshold slope(ss) of 78mV/dec

Effective electron mobility (μ_{eff}) between de-

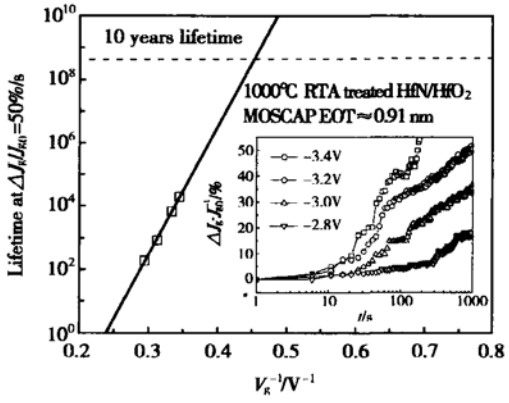


Fig. 7　Lifetime projection based on SILC of HfN/HfO_2 MOSCAP after 1000℃ PMA with EOT = 0.91nm　Failure criterion is set at 50% increment of J_{g_0}. Inset shows typical SILC time evolutions at four gate voltages.

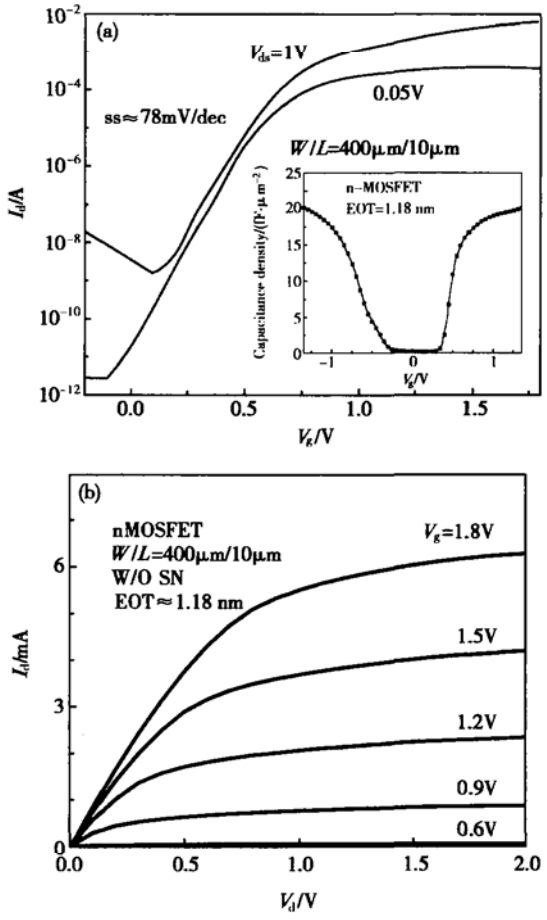


Fig. 8　(a) I_d-V_g characteristics of a n-MOSFET using HfN/HfO_2 gate stack (W/O surface nitridation) with EOT ≈ 1.18nm　The inset shows HFCV measurement of the n-MOSFET; (b) I_d-V_d characteristics from the corresponding n-MOSFET

vices with and without SN is compared in Fig. 9(a), where the μ_{eff} is measured by the split C-V method[18]. It is seen that the electron mobility is degraded in the SN device despite its larger EOT, which is attributed to the larger interface trap density (D_{it}) due to nitrogen incorporation at the HfO_2/Si, as shown in Fig. 9(b) where D_{it} is measured by the direct-current current-voltage (DCIV) technique[19], using interface trap capture cross section of 0.044nm^2[20].

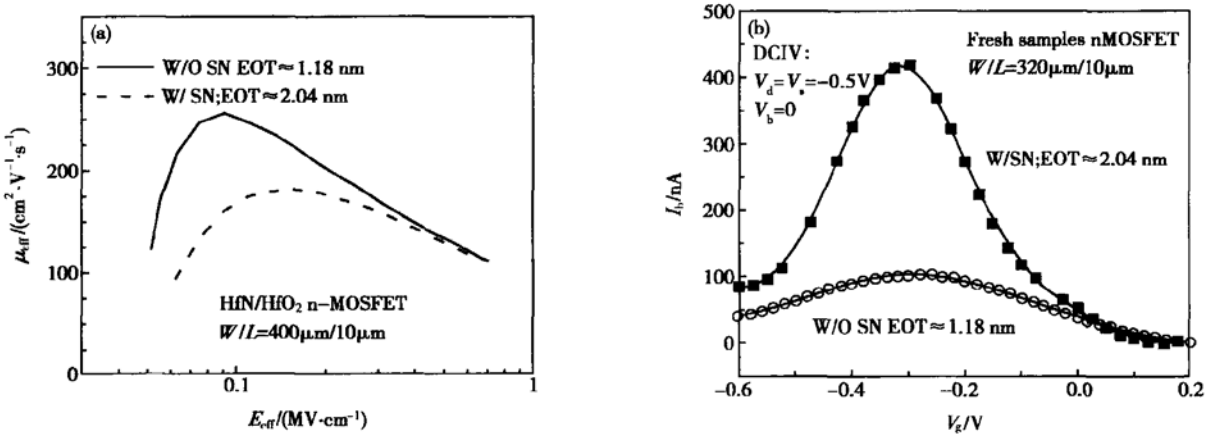


Fig. 9 (a) SN treatment effect on effective electron mobility for HfN/HfO_2 MOSFETs The effective electron mobility is degraded for SN device despite the larger EOT. (b) DCIV measurement show that interface trap density D_{it} is ~ $3\times10^{11}/cm^2$ for fresh SN n-MOSFET (EOT ≈ 2.04nm), and D_{it} ~ $7\times10^{10}/cm^2$ for fresh device W/O SN with EOT ≈ 1.18nm.

4 A dual-metal gate integration process for CMOS with sub-1nm EOT HfO_2 by using HfN replacement gate

Figure 10 illustrates a simplified process flow of the proposed HfN replacement gate process. The feasibility of this process was demonstrated using MOS capacitors. First, the devices with the HfN/HfO_2 gate stack were fabricated. The process details could be found in the last section of this paper. After gate patterning, all the devices were subjected to RTA in N_2 at 1000℃ for 20s, which is adequate for source/drain dopant activation. The TaN/HfN dummy stack on some devices was then removed by standard cleaning-1(SC-1) (NH_4OH+ H_2O_2+ H_2O) and diluted hydrofluoric acid (DHF) (1∶100) solutions, respectively. It should be noted that the SC-1 solution does not attack the HfN metal. Finally, a layer of Ta, Ni, or HfN (~ 100nm) was deposited on the exposed HfO_2 gate dielectric to form the new gate electrodes. In the end, Al metallization and FGA at 420℃ were performed to complete the devices. C-V and I-V characteristics were then measured. The EOT and V_{fb} values were determined from the measured C-V curves.

In last section, we have successfully demonstrated that the EOT of the HfN/HfO_2 gate stack was scaled down to less than 1nm after 1000℃ RTA annealing. The transistor electrical characteristics are reported elsewhere[21]. However, the work function of HfN is close to the mid-gap level of silicon. In this work, by replacing the HfN dummy gate with Ta or Ni, dual-metal gates with work functions satisfying the required values for bulk CMOS transistors can be realized while maintaining a high quality sub-1nm HfO_2 gate dielectric.

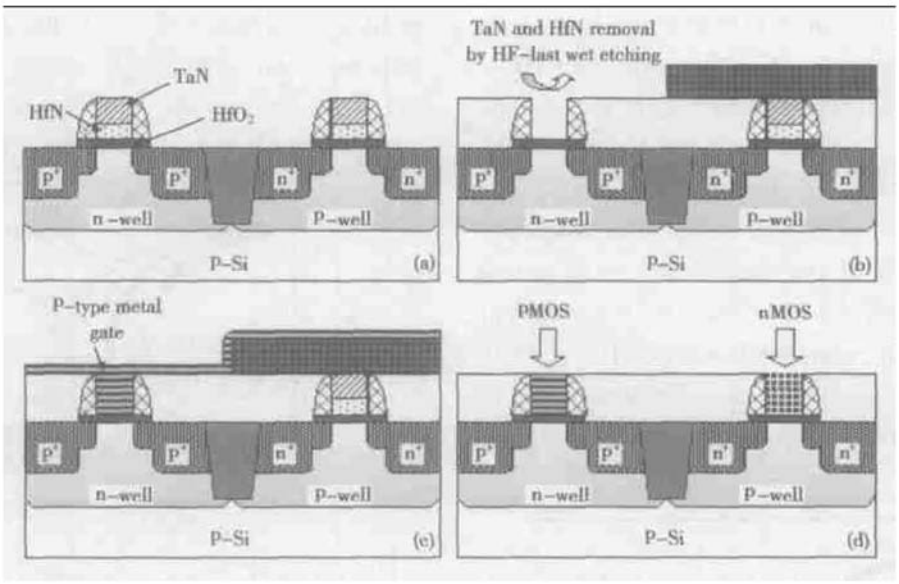


Fig. 10　Schematic of the dual-metal gate CMOS integration flow employing HfO_2 dielectric and HfN replacement gate, showing the formation of HfN/HfO_2 gate stack(a), selective removal of HfN dummy gate (b), formation of PMOS metal gate(c), and formation of NMOS metal gate(d)

Figure 11 compares the etch rates of HfN and HfO_2 by DHF solution. The etch rate of HfN is around 12nm/min while that of HfO_2 after 1000℃ PDA is almost negligible. This demonstrates the high etch selectivity of the HfN over HfO_2 using DHF solution. Figure 12 examines the surface morphology of the HfO_2 film using atomic force microscopy (AFM) under three different conditions:

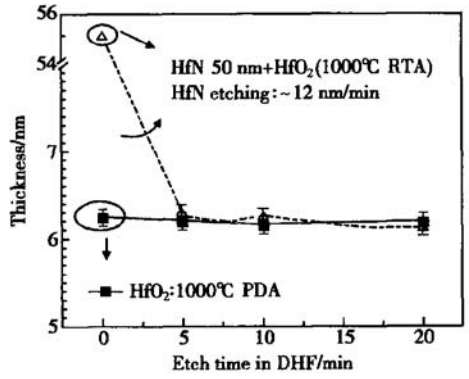


Fig. 11　Thickness variation of the HfN/HfO_2 gate stack (open symbol) and HfO_2 (solid symbol) versus etch time in diluted HF solution (1∶100), demonstrating the high etch selectivity of HfN with respect to HfO_2. The etch rate of HfN and the thickness of HfO_2 are determined by surface profiler and ellipsometer, respectively.

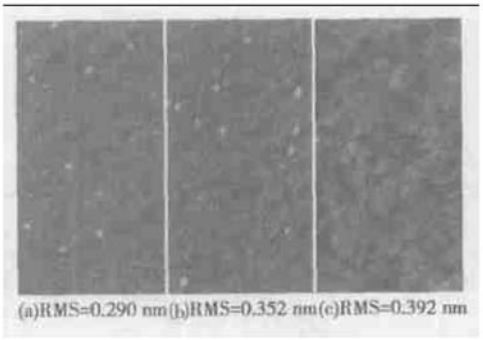


Fig. 12　AFM pictures for HfO_2 surfaces obtained from as-deposited film(a), after 1000℃ RTA anneal (b), and 1000℃ RTA followed by HfN etching in DHF solution for 6min(c)

as-deposited HfO_2 film, HfO_2 after 1000℃ RTA anneal, and HfO_2 in HfN/HfO_2 stack with HfN removed by DHF solution after 1000℃ RTA anneal. The root mean square (RMS) roughness variation induced by the DHF etching process is about 0.05nm, indicating that there is negligible physical damage to the HfO_2 film during the HfN etch process. To further examine any potential impacts on the electrical properties of HfO_2, a new HfN metal layer was re-deposited onto HfO_2 dielectric after removing the HfN dummy gate. Figures 13 (a) and (b) compare the C-V and I-V characteristics of the

control HfN/HfO_2 devices (1000℃ anneal, without HfN removal process) and the re-deposited HfN/HfO_2 devices (with re-deposited HfN gate). The identical EOT (~ 0.8nm) and gate leakage of the devices suggest that the ultra-thin HfO_2 film is not physically and electrically damaged. The small difference in the V_{fb} of the control and re-deposited HfN/HfO_2 devices could be due to the different thermal treatment employed on the HfN gate in these two groups of devices, and the dependence of metal gate work function on anneal temperature[22].

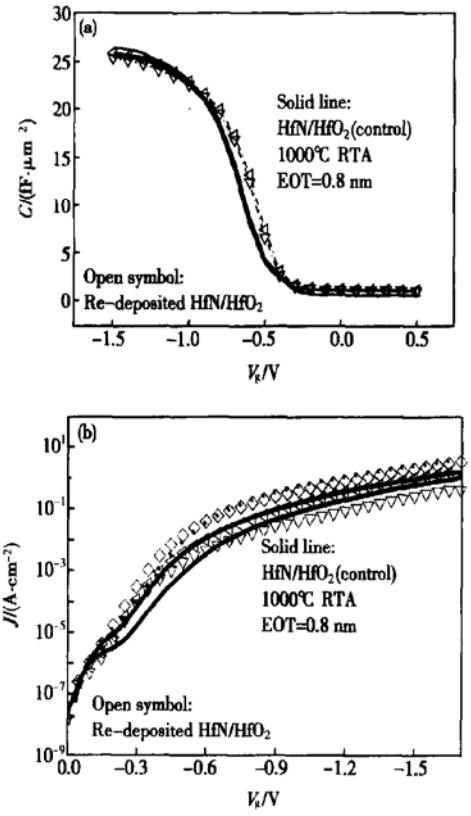


Fig. 13 C-V (a) and I-V (b) characteristics of the control HfN/HfO_2 devices and re-deposited HfN/HfO_2 devices with HfO_2 EOT ≈0.83nm

The above results suggest that HfN could be used as a dummy gate material on HfO_2 in a replacement gate process. In this work, Ta and Ni are used to replace HfN for NMOS and PMOS transistors, respectively. Figure 14(a) shows the high frequency C-V measurements for the Ta-gate/HfO_2 and Ni-gate/HfO_2 devices using the HfN replacement gate process. The C-V hysteresis of all the devices is less than 20mV, which could be due to the high-temperature annealing effect applied to the HfN/HfO_2 gate stack. The C-V measurements

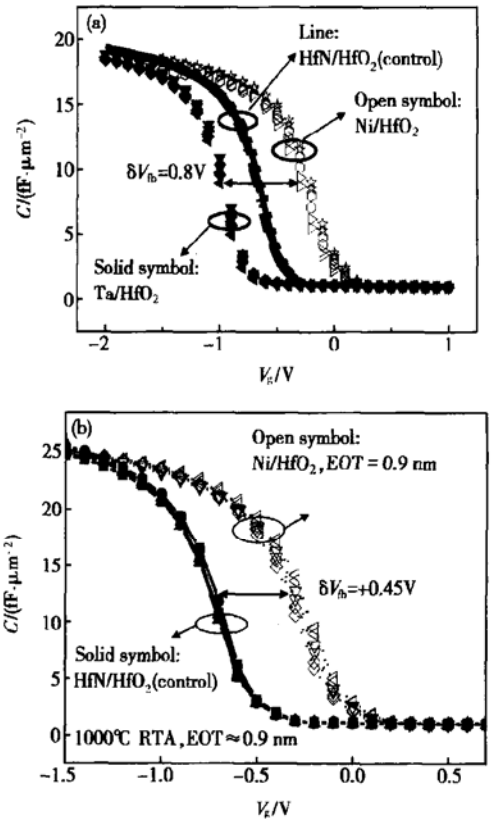


Fig. 14 (a) High frequency C-V curves of the HfN/HfO_2 control devices and re-deposited Ta/HfO_2, Ni/HfO_2 devices with a same EOT; (b) High frequency C-V characteristics of the re-deposited Ni/HfO_2 devices with ultra-thin (EOT ≈0.9nm) HfO_2 and remarkable V_{fb} shift (+0.45V)

of all the devices fit well with the simulation curves, indicating negligible changes in the HfO_2/Si interface quality during the HfN removal process. The work function shifts attributed to Ta and Ni with respect to HfN are −0.35eV and +0.45eV, respectively. The work function difference of 0.8eV between the gate electrodes of bulk NMOS and PMOS transistors could be adequate for good device performance. For the re-deposited Ni-gate/HfO_2 devices, ultra-thin EOT (~ 0.9nm) is also achieved (Fig. 14(b)) without degradation to the gate leakage (Fig. 15(b)). Figures 15(a) and (b)

compare the TDDB and the gate leakage characteristics of the re-deposited HfN/HfO_2, Ta/HfO_2, and Ni/HfO_2 devices with the HfN/HfO_2 control devices. It is observed that the gate leakage of Ta/HfO_2 (or Ni/HfO_2) devices is slightly higher (or lower) than that of the HfN/HfO_2 control devices. This can be attributed to the lower (or higher) work function of Ta (or Ni) compared to HfN. The TDDB characteristics obtained using constant current stress (CCS) are also compared among the control HfN/HfO_2 devices and all the devices with re-deposited metal gates on HfO_2 (EOT = 1.35nm). No significant degradation is observed after the HfN replacement gate process, as shown in Fig. 15(a). Additionally, this HfN replacement gate process can also be applied for integration of other metal gate candidates, besides Ta and Ni, in a CMOS process employing sub-1nm EOT HfO_2 gate dielectric.

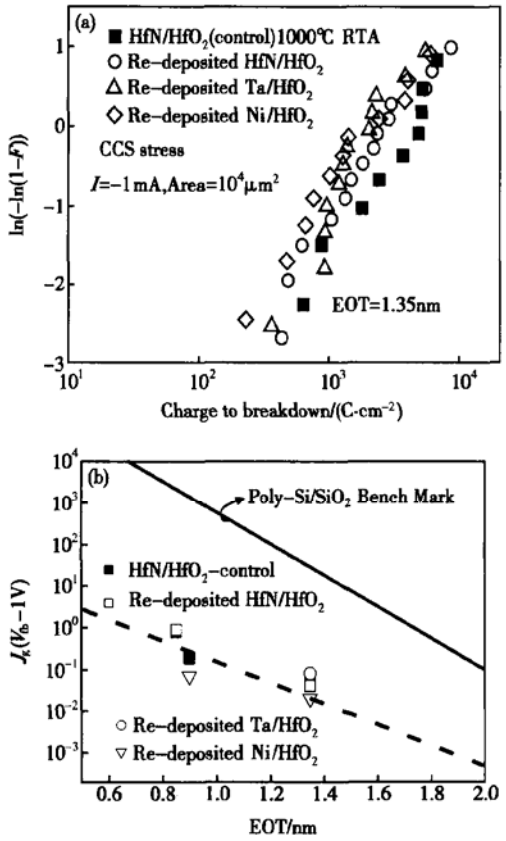


Fig. 15　Comparison of TDDB (a) and gate leakage (b) characteristics between the control HfN/HfO_2 devices and re-deposited HfN/HfO_2, Ta/HfO_2, Ni/HfO_2 devices　CCS was performed at a current density of ~ 8A/cm^2 on devices with an area of 100μm × 100μm at room temperature. Figure 15(b) shows the leakage data from the two different sets of devices with different EOTs.

5 Conclusion

In conclusion, we report the material and electrical properties of HfO_2 high-k gate dielectric. In the first part, the band alignment of ALD $(HfO_2)_x(Al_2O_3)_{1-x}$ to (100) Si substrate and thermal stability of $(HfO_2)_x(Al_2O_3)_{1-x}$ are studied. XPS valence band spectra, and O 1s energy loss spectra show continuous changes with the variation of Hf(Al) composition in $(HfO_2)_x(Al_2O_3)_{1-x}$. E_g and ΔE_v values for $(HfO_2)_x(Al_2O_3)_{1-x}$ on Si(100) are determined and can be expressed by $6.52-1.27x$ (eV), and $3.03-0.81x$ (eV), respectively. The thermal stability of Hf aluminates and its impact on oxygen diffusivity through Hf aluminates are also studied by TEM and XPS. Our results show that both the thermal stability and the resistance to oxygen diffusion of HfO_2 are improved by adding Al to form Hf aluminates, and the improvement is closely correlated with the Al percentage in the films. In the second part, thermally robust high quality HfN/HfO_2 gate stack is demonstrated for advanced MOS device applications. Due to the superior oxygen diffusion barrier of HfN as well as the thermal stability of HfN/HfO_2 interface, EOT of HfN/HfO_2 gate stack has been successfully scaled down to less than 1nm with excellent leakage, and long-term reliability even after 1000℃ PMA, without using SN prior to HfO_2 deposition. Negligible variation in both the EOT and the work function of HfN/HfO_2 gate stack are observed upon PMA treatments up to 1000℃. The last part of the paper demonstrates a novel HfN replacement gate process as a simple approach for integrating dual-metal gates in CMOS transistors with sub-1nm HfO_2 gate dielectric. The excellent thermal stability of the HfN/HfO_2 gate stack and the high etch se-

lectivity between HfN and HfO_2 allows the achievement of an ultra-thin, damage-free, low leakage HfO_2 gate dielectric with good TDDB characteristics using a replacement gate process. Ta and Ni replacement metal gate electrodes are successfully demonstrated, achieving a work function difference of about 0.8eV between the NMOS and PMOS gate electrodes.

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