第 25 卷第 10 期　　半 导 体 学 报　　Vol. 25, No. 10
2004 年 10 月　　CHINESE JOURNAL OF SEMICONDUCTORS　　Oct., 2004

A Novel Technique of Parameter Extraction for Short Channel Length LDD MOSFETs*

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Abstract: A novel parameter extraction technique suitable for short channel length lightly-doped-drain (LDD) MOSFET's is proposed which segments the total gate bias range, and executes the linear regression in every subsections, yielding the gate bias dependent parameters, such as effective channel length, parasitic resistance, and mobility, etc. This method avoids the gate bias range optimization, and retains the accuracy and simplicity of linear regression. The extracted gate bias dependent parameters are implemented in the compact I-V model which has been proposed for deep submicron LDD MOSFET's. The good agreements between simulations and measurements of the devices on 0.18μm CMOS technology indicate the effectivity of this technique.

Key words: LDD MOSFET; parameter extraction; parasitic series resistance; mobility
PACC: 7220H; 7230　　**EEACC**: 2560B; 2560R
CLC number: TN386　　**Document code**: A　　**Article ID**: 0253-4177(2004)10-1215-06

1 Introduction

The device parameter extraction is important for describing the device electrical characteristics in CMOS technology. The linear regression extraction is one of the most effective methods. However, it is not easy for very short channel devices because the fundamental assumption of the linear R_{total}-V_{gt}^{-1} derived from the measured I_{ds}-V_{gs} curves causes significant errors, particularly for the lightly-doped-drain (LDD) devices. Many improved extraction methods, such as "S&R" method, "single device" method, etc., have been published for this purpose[1~5]. As a matter of fact, some of parameters, including electrical effective channel length, parasitic series resistance, mobility, etc., are gate bias dependent, although artificially constant L_{eff} and R_{ds} are more desirable for compact model. Thus an optimized gate overdrive (V_{gt}= V_{gs}- V_{th}) range has to be determined for linear regression operations in order to minimize the bias dependence of the parameters, which is usually technology specific. This is why most extraction techniques require a similar gate bias range optimization[1~5]. With the decreases of channel length and gate oxide thickness, the obvious nonlinearity that is caused by the effect of the gate voltage on the channel electric field through very thin gate oxide increases the difficulties of this work.

This paper presents a new extraction method in which the total gate bias range is segmented into many small bias subsections, and then the linear regression is executed in every bias subsection, which results in the bias independent parameters . The different values of the parameters are obtained at different gate bias subsections. In other words, the

* Project supported by National Natural Science Foundation of China(No. 60206006)
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Received 22 December 2003, revised manuscript received 29 March 2004

gate bias dependent parameters are derived. This simple method avoids the complicated optimization of the gate bias range and retains the accuracy of linear regression extraction. As validity, the measured data from LDD NMOSFETs of different channel lengths fabricated on 0.18μm LDD CMOS technology are used to extract the gate bias dependent L_{eff}, R_{ds}, and μ_{eff} with the new method, and then these parameters are implemented in the compact model which has been proposed for short channel LDD MOSFETs.

2 Parameter extraction technique

In the theory of linear regression extraction, at a very small drain bias (approximately V_{ds} = 50mV), the total drain to source resistance is expressed by[5]

$$R_{total} = \frac{V_{ds}}{I_{ds}} = R_{ds} + \frac{L_{mask} - \Delta L}{\mu_0 C_{ox} W} \times \left(\frac{1}{V_{gt}} + \theta\right) \tag{1}$$

where R_{ds} is parasitic series resistance outside the channel, $L_{eff} = L_{mask} - \Delta L$ equals electrical effective channel length and ΔL is defined as the channel reduction, the gate overdrive $V_{gt} = V_{gs} - V_{th}$ and V_{th} is the threshold voltage, C_{ox} and W are the gate oxide capacitance and the gate width, respectively, μ_0 and θ are the low electric field mobility and the mobility degradation factor, respectively. The linearity between R_{total} and V_{gt}^{-1} must be guaranteed in linear regression operation, therefore the gate bias independent parameters μ_0, θ and ΔL must be assumed. It is also shown from Eq. (1) that the relation between R_{total} and L_{mask} is linear at a constant gate bias, thereby for R_{ds} and θ extraction of devices with different channel lengths. In fact, the nonlinearity between R_{total} and V_{gt}^{-1} is clearly shown in short channel length and very thin gate oxide devices, even in a small gate bias range. In our work, the LDD NMOSFETs with 3.2nm gate oxide thickness and different gate lengths on 0.18μm CMOS technology give the R_{total}-V_{gt}^{-1} curves shown in Fig. 1. These curves demonstrate the serious nonlinearity at the range of total bias V_{gt} that should be just used for extraction. This phenomenon indicates that some of the extracted parameters are closely gate bias dependent[3] particularly for LDD devices. This in turn causes a problem of accuracy of linear regression.

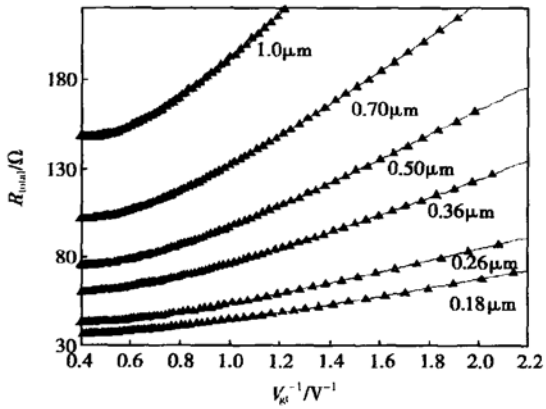

Fig. 1 Drain-source resistance versus V_{gt}^{-1} nonlinear curves derived from the I_{ds}-V_{gs} characteristics of different gate length LDD NMOSFETs with thin gate oxide(3.2nm) and 20μm gate width fabricated on 0.18μm CMOS technology

However, the simplicity of the linear regression extraction is an attractive issue in device modeling. It is hence proposed in this paper that the related parameters are treated as gate bias independent in a very small gate bias range, such as 0.1V range, therefore guaranteeing the effectivity of linear regression. The total V_{gt} range is segmented by 0.1V step and the linear regression extraction is repeated in different subsections to obtain the parameter array at different gate biases. It is noted that the subsection range which is average of 0.1V in this paper is determined in terms of the nonlinearity of R_{total}-V_{gt}^{-1} characteristic, that is, the large range for weekly nonlinearity, and the small for strong nonlinearity, usually a factor lower than the total V_{gt} range. The smaller range will improve the description of the bias dependence, and yet increase the calculations. Consequently, the extracted $R_{ds}(V_{gt})$ and the $\Delta L(V_{gt})$ are modeled by curve fit-

ting in order to implement in the device model. Simultaneously, the extracted μ_0 and θ give the effective mobility $\mu_{eff}(V_{gt})$ array by $\mu_{eff}=\mu_0/(1+\theta V_{gt})$. In our work, the LDD NMOSFETs with 0.18~2.0μm gate mask lengths are used to extract the parameters by linear regression. In details, the threshold voltages V_{th} of different L_{mask} devices are first extracted by "peak g_m" technique from the measured I_{ds}-V_{gs} characteristics and then the gate overdrive V_{gt} is obtained for next extraction operation. For every device of different gate length L_{mask}, at each 0.1V step of V_{gt}, the slope of R_{total}-V_{gt}^{-1} straight line, i.e., slope$=(L_{mask}-\Delta L)/\mu_0 C_{ox} W$, is obtained and then is used to plot the slopes-L_{mask} curve which should be straight line under the assumption of gate bias independent parameters. By linear regression, the slope of the straight line (it equals $1/\mu_0 C_{ox} W$) is used to extract μ_0 and the intercept of the line gives ΔL. Simultaneously, a family of R_{total}-L_{mask} straight lines at different V_{gt}^{-1} biases is drawn, and then be used to extract R_{ds} by intercept with the vertical line of ΔL while the ΔL has been determined. Different from the R_{ds} extraction and interpretation in Ref. [5], the well linearized family of R_{total}-L_{mask} lines must intersect at one point with a coordinate $(\Delta L, R_{ds})$, which is easily understood from Eq. (1). This point gives the R_{ds} independent with V_{gt}. Furthermore, the θ is extracted by slope of the R_{total}-L_{mask} straight line at extrapolated $V_{gt}^{-1}=0$, i.e., slope$=\theta/\mu_0 C_{ox} W$. The μ_0 and θ are then used to derive the effective mobility μ_{eff}. Finally, the linear regression operations step by step yield the R_{ds}-V_{gt}, the ΔL-V_{gt}, and the μ_{eff}-V_{gt} curves. These accurate extraction parameters are then embedded in the compact model of the devices. In the device model, a constant low electric field mobility μ_0 and a constant mobility degradation factor θ are more desired. To this end, the μ_{eff}-V_{gt} curve is used to optimize the two constants by least square algorithm at the total bias range, shown as[6]

$$\mu_{eff}=\frac{\mu_0}{1+\theta V_{gt}^r} \tag{2}$$

where the factor r indicates the nonlinearity of the curve. To obtain the physically reasonable constant μ_0 and θ, the factor r is not unity and related with process for short channel length LDD devices, which has been experimentally proved in Refs. [6, 7]. The optimized results in our work will be illustrated in next section.

3 Experiment and extraction results

The extraction is operated on an array of LDD NMOSFETs with 20μm gate width and 0.18, 0.26, 0.36, 0.5, 0.7, 1.0, 1.5, and 2.0μm gate lengths, on 0.18μm CMOS technology and the gate oxide thickness is 3.2nm. By "peak g_m" technique, the extracted threshold voltages of different gate lengths are shown in Fig. 2(a), in which the V_{th} reduction is observed in very short channel length devices. By continuous linear regression, the extracted R_{ds}, ΔL, and μ_{eff} curves at 0.2~2.5V gate overdrive V_{gt} range are demonstrated in Fig. 2(b)~(d). The results indicate that it would cause big errors if the gate bias independent parameters were assumed in compact device model. It is also found in the figures that R_{ds} and ΔL decrease from maximum and tend to be constants with the V_{gt} increasing to high value. This indicates that the bias independent parameter's assumption is practical when the V_{gt} is high enough. This is why the constant parameters are usually assumed in large dimensional devices with high bias voltage operations. But this is limited by the low bias applications in deep submicron devices, increasing the difficulties of the parameter extractions. In Fig. 2(d), the well optimized curve gives the results: $\mu_0=307\text{cm}^2/(\text{V}\cdot\text{s})$, $\theta=0.16$, and $r=1.65$. They are in reasonable range. The low μ_0 value is caused by the t_{ox}, very small gate oxide thickness. It has been illustrated experimentally in Ref. [4] that the reduced t_{ox} yields the decreased mobility.

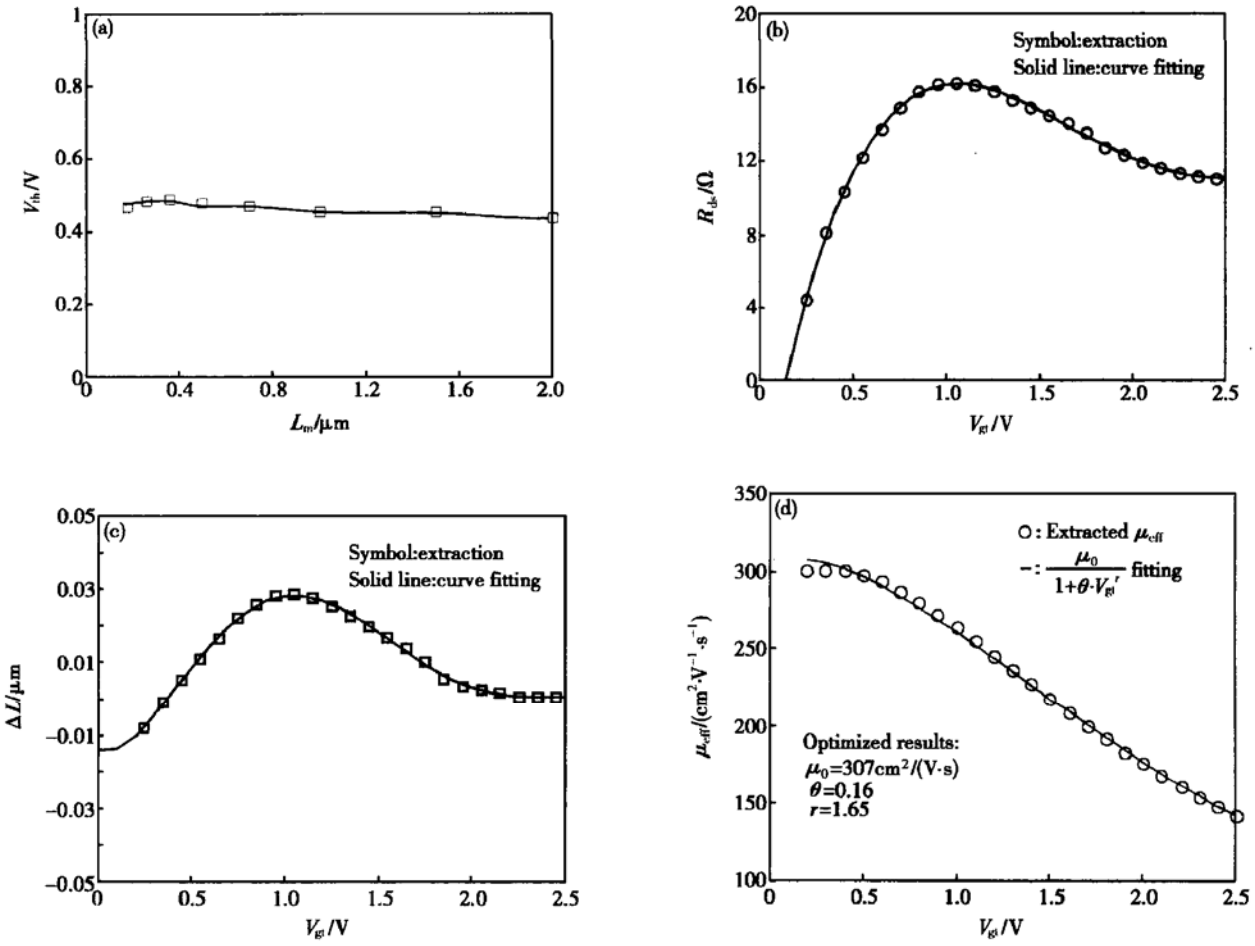

Fig. 2 Extracted parameters by new method, where (a) is the extracted threshold voltages of different gate length LDD NMOSFETs by "peak transconductance and extrapolation" method, (b) is the gate bias dependent parasitic series resistance, (c) is the gate bias dependent channel reduction, and (d) is the gate bias dependent effective mobility. The solid line in (d) is the optimized result which gives the constant μ_0 and θ for device model.

4 Validity in the LDD nMOSFET's *I*–*V* model

The extracted parameters are implemented in the LDD nMOSFET's compact *I*–*V* model which has been proposed and detailed in Ref. [8], briefly given as follows.

The nonlinear current $I_{ds}(V_{gs}, V_{ds})$ with hyperbolic-tangent description is given by

$$I_{ds}(V_{gs}, V_{ds}) = I_{dsat}(1 + \lambda V_{ds})\tanh(\alpha V_{ds}) \quad (3)$$

where the critical saturated drain current I_{dsat}, the channel length modulation parameter λ, and the saturation voltage parameter α are given respectively as

$$I_{dsat} = W v_{sat} C_{ox}(V_{gs} - V_{th} - \gamma V_{dsat}) \quad (4)$$

$$\lambda = \frac{\frac{\partial I_{ds}}{\partial V_{ds}}\Big|_{V_{ds} \geqslant V_{dsat}}}{I_{dsat}} = \frac{1}{V_{ds}} \times \frac{l_d E_c}{(L_{eff} - l_d)E_c + V_{dsat}}, \quad V_{ds} > V_{dsat} \quad (5)$$

$$\alpha = \frac{\frac{\partial I_{ds}}{\partial V_{ds}}\Big|_{V_{ds} \to 0}}{I_{dsat}} = \frac{1}{I_{dsat}} \times \xi \frac{\mu_s C_{ox} W}{L_{eff}} \times (V_{gs} - V_{th} - \gamma V_{ds}), V_{ds} < V_{dsat} \quad (6)$$

The process well matched substrate current model for submicron and deep-submictron LDD MOSFETs is shown as

$$I_{sub} = I_{ds} \times \frac{A_i}{B_i} \times (V_{ds} - \eta V_{dsat}) \times \exp\left(-\frac{l B_i}{V_{ds} - \eta V_{dsat}}\right) \quad (7)$$

In this model, R_{ds} (i.e. $R_d + R_s$) is defined as external parameter, and the relation between external

and intrinsic biases yields an iterated calculation for the model. So the extracted R_{ds} and ΔL fitting models are easily embedded to the I–V characteristics. It is clear that the gate bias dependent parasitic series resistance and channel reduction are more reasonable for describing the reality of device. The simulated and experimental characteristics families of 20μm/0.18μm LDD NMOSFET, including I_{ds}–V_{ds}, I_{ds}–V_{gs}, g_m–V_{gs}, and I_{sub}–V_{gs}, are given

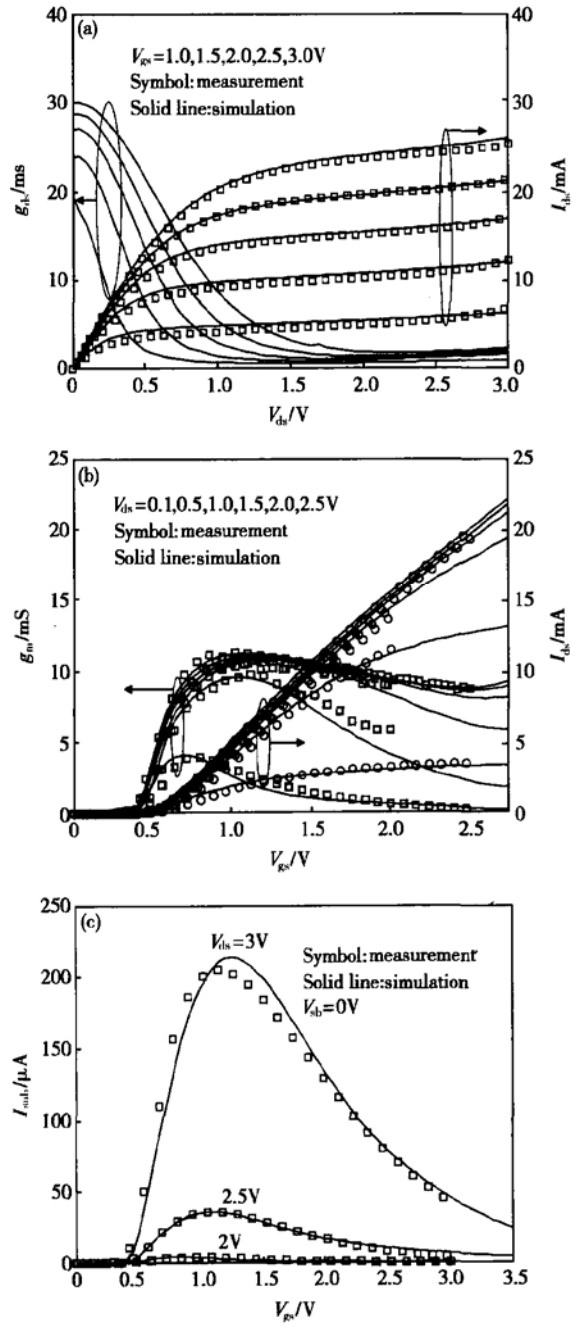

Fig. 3　Measured and simulated characteristics of 20μm/0.18μm LDD NMOSFETs, where (a) is the output drain current characteristics and drain conductance, (b) is the I_{ds} versus V_{gs} characteristics and the transconductance including linear and saturation regions, and (c) is the substrate current characteristics at zero substrate bias

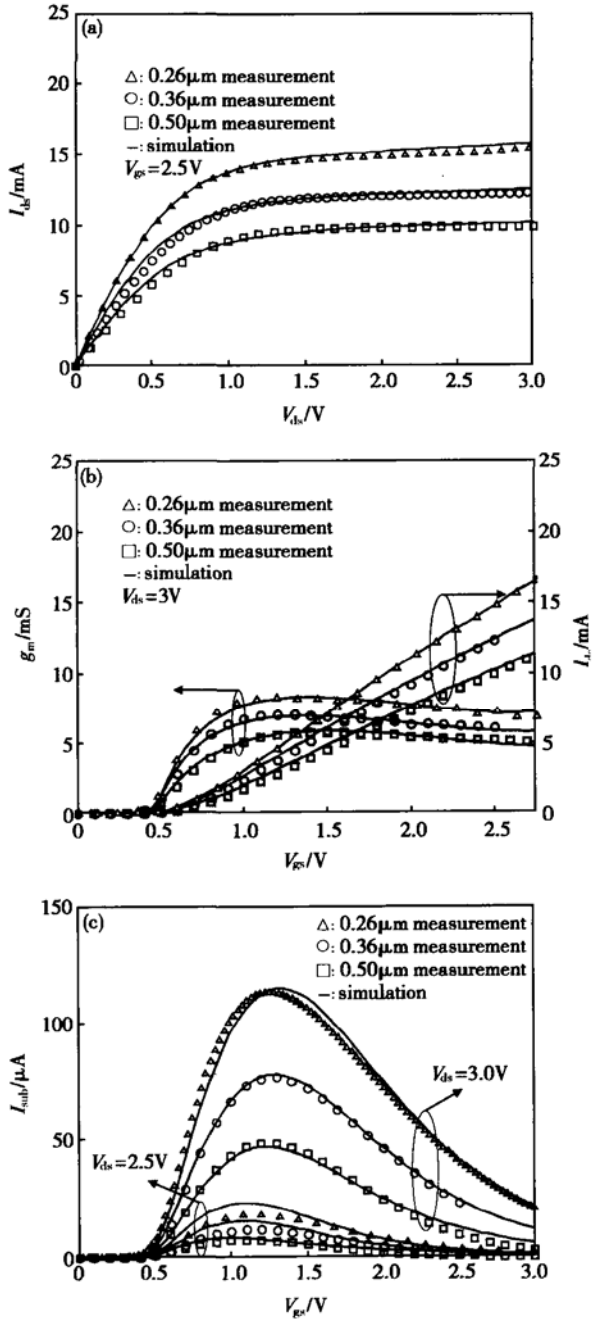

Fig. 4　Measured and simulated characteristics of 20μm/0.26, 0.36μm and 0.50μm LDD NMOSFETs, where (a) are the output drain currents, (b) are the I_{ds}–V_{gs} characteristics including transconductances, and (c) are the substrate currents(V_{sb}= 0V)

in Fig. 3(a) ~ (c). The excellent agreements between simulations and measurements show the accuracy of the extracted parameters and the effectivity of the compact I-V model for deep submicron devices. Furthermore, Figure 4(a) ~ (c) also give the comparison between measurements and simulations of 0.26, 0.36, and 0.5μm gate lengths LDD devices. The results indicate the robustness of the extraction technique and the device model.

5 Conclusion

We propose a novel parameter extraction technique suitable for short channel length LDD MOSFET's. It avoids the gate bias range optimization of the linear regression extraction by segmenting the total gate bias region. In a very small gate bias range, the extracted parameters are nearly gate bias independent, therefore maintaining the effectivity of linear regression. The repeat extraction operations accurately obtain the gate bias dependent parameters and well be modeled. The extracted parameters are then implemented in the proposed I-V model for LDD MOSFET's. The agreements between simulations and measurements of different gate lengths' devices indicate the effectivity and the robustness of this technique.

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一种适用于短沟道 LDD MOSFET 参数提取的改进方法*

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摘要: 提出了一种适用于短沟道 LDD MOSFET 的改进型参数提取方法, 通过对栅偏压范围细分后采用线性回归方法, 提取偏压相关参数, 保证了线性回归方法的精度和有效性, 避免了对栅偏压范围的优化和误差考虑. 提取出的参数用于已建立的深亚微米 LDD MOSFET 的 I-V 特性模型中, 模拟与测试数据的吻合表明了该方法的实用性.

关键词: 轻掺杂漏 MOSFET; 参数提取; 寄生串联电阻; 迁移率

PACC: 7220H; 7230 **EEACC**: 2560B; 2560R

中图分类号: TN386 **文献标识码**: A **文章编号**: 0253-4177(2004)10-1215-06

* 国家自然科学基金资助项目(批准号: 60206006)

于春利 女, 博士研究生, 从事深亚微米 CMOS 器件建模及可靠性应用的研究.

2003-12-22 收到, 2004-03-29 定稿