第 25 卷第 10 期　　半 导 体 学 报　　Vol. 25, No. 10
2004 年 10 月　　CHINESE JOURNAL OF SEMICONDUCTORS　　Oct., 2004

Strained Si Channel Heterojunction pMOSFET Using 400℃ LT-Si Technology*

Mei Dinglei[1], Yang Mohua[1], Li Jingchun[1], Yu Qi[1], Zhang Jing[2], Xu Wanjing[2] and Tan Kaizhou[2]

(1 *School of Microelectronics and Solid-State Electronics, University of Electronic Science and Technology of China, Chengdu* 610054, *China*)

(2 *National Key Laboratory of Analog IC's, Chongqing* 400060, *China*)

Abstract: A novel MBE-grown method using low-temperature (LT) Si technology is introduced into the fabrication of strained Si channel heterojunction pMOSFETs. By sandwiching a low-temperature Si layer between Si buffer and SiGe layer, the strain relaxation degree of the SiGe layer is increased. At the same time, the threading dislocations (TDs) are hold back from propagating to the surface. As a result, the thickness of relaxed $Si_{1-x}Ge_x$ epitaxy layer on bulk silicon is reduced from several micrometers using UHVCVD to less than 400nm ($x = 0.2$), which will improve the heat dissipation of devices. AFM tests of strained Si surface show RMS is less than 1.02nm. The DC characters measured by HP 4155B indicate that hole mobility μ_p has 25% of maximum enhancement compared to that of bulk Si pMOSFET processed similarly.

Key words: SiGe; low-temperature Si; strain relaxation; threading dislocation

EEACC: 2560R

CLC number: TN386　　**Document code**: A　　**Article ID**: 0253-4177(2004)10-1221-06

1 Introduction

With years of inspiring developments, Si-CMOS devices have been progressed into sub 0.1μm regime by aggressive scaling. However, as dimensions continue to shrink, device scaling is becoming increasingly difficult due to various physical and technological limitations[1].

In searching propellants for the next generation of microelectronic devices and integrated circuits, channel engineering has been attracting more and more attention, which enhances carrier transport in the MOSFET channel by its material properties changed. Today silicon germanium (SiGe) used as either channel material or relaxed virtual substrate is the most promising choice. Grown by ultra high vacuum chemical vapor deposition (UHVCVD), several micrometers composition grading SiGe layer can achieve nearly fully relaxed SiGe with threading dislocation density less than $10^6 cm^{-2}$[2]. When Si is grown on relaxed $Si_{1-x}Ge_x$, it will be strained with type Ⅱ band alignment, which will increase both the electron and hole mobility. Based on this technology, both hetero-nMOSFETs and pMOSFETs show better performances than that of similarly processed bulk-Si n/p MOSFETs[3,4].

However, this composition grading technology has several drawbacks.

* Project supported by Funds National Key Laboratory of Analog IC (No. 2000JS09.3.1.DZ02)

Mei Dinglei male, was born in 1981. His research subject is mainly about SiGe CMOS device and circuit. Email: meidinlei@std.uestc.edu.cn

Received 25 December 2003, revised manuscript received 8 May 2004

(1) Due to strain relaxation of SiGe alloy, threading dislocation density are dramatically influenced by the composition-grading rate. Higher Ge fraction requires thicker layer, which is unfavorable for heat dissipation of devices and mass fabrication in industry due to its high cost.

(2) The SiGe epitaxy layers, grown by UHVCVD, usually suffer from surface fluctuation with amplitude in a range of 15~ 20nm, which adds difficulties in the growth of upper layers.

To overcome these drawbacks, several technologies for ultra-thin virtual SiGe substrates are developed, such as low-temperature (LT) Si or SiGe technology[5], LEPECVD technology[6], hydrogen or helium ion implantation technology[7]. In this paper, 400℃ LT-Si technology is employed in fabricating strain-Si pMOSFET.

2 Device structure

The cross section of strained Si heterojunction pMOSFET is shown in Fig. 1.

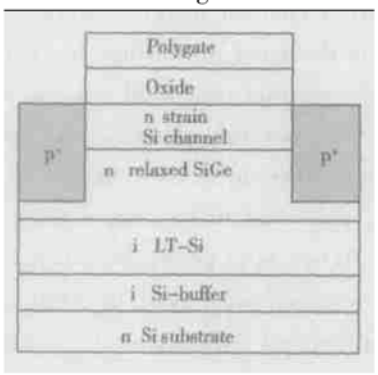

Fig. 1 Designed cross section of the strained Si channel pMOSFET with gate length $L = 4.5\mu m$

All layers beyond the n-Si substrate are grown by MBE, which will be discussed in details later. After low temperature oxidation of surface strained Si layer, 11nm gate oxide is formed. The thickness of N^+ doped polysilicon gate is 480nm. Shown in Fig. 2 and measured precisely by scanning electronic microscope(SEM), the width and the length of the device are 52μm and 4.5μm, respectively.

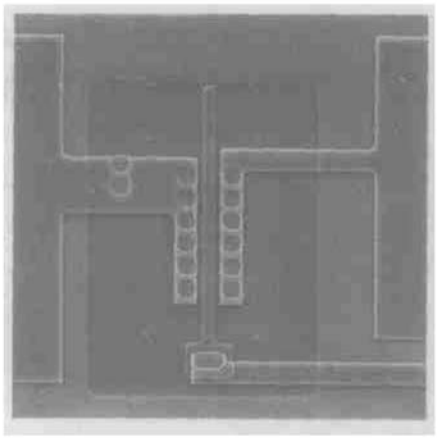

Fig. 2 SEM photo of the strained Si channel pMOSFET with $W/L = 52\mu m/4.5\mu m$

3 Experiment

The whole layers are grown on φ100mm 〈100〉 n-type Si substrate by solid source MBE, shown in Fig. 3. The Si buffer layer grown directly on Si substrate can separate overgrown layer from surface damages on Si substrate, introduced by CMP etc. In our experiment 10nm Si buffer grown at 700℃ is used. With LT-Si technology employed, a 100nm LT-Si layer grown at 400℃ is sandwiched between 300nm SiGe layer and 10nm Si buffer layer. The point defects introduced by this layer can enhance the relaxation degree of upper layers and hold back threading dislocations from propagating to the surface. Still there may be remaining strain in the early grown SiGe layer. However, as the layer thickness is approaching to 300nm, the strain caused by crystal lattice mismatch of $Si_{1-x}Ge_x$/Si hetero structure can be relieved. In the end, the $Si_{1-x}Ge_x$ layer is fully relaxed. When 12nm n-Si and 5.3nm i-Si are grown, they are strained. The top 5.3nm i-Si is sacrificial layer for gate oxidation. Results from oxidation experients show that due to stretching strain in surface layers, the oxidation rate is much lager than that of bulk silicon. This adds difficulties to control precisely the oxidation thickness and to maintain the process stability.

5.3nm	i	strained Si
12nm	n	strained Si
300nm	n	relaxed $Si_{0.8}Ge_{0.2}$
100nm	i	LT-Si
10nm	i	Si buffer
n Si sub ⟨100⟩ 1~ 5Ω/□		

Fig. 3　Total structure of epitaxy layers of strained Si channel pMOSFET

After growth of strained Si/relaxed SiGe layers, the heterojunction MOSFETs are fabricated with standard CMOS fabrication process, except for the gate oxidation and annealing.

If the oxidation temperature is too high, Ge diffuses into channel, which will change the strained Si to strained $Si_{1-y}Ge_y$ ($0 < y < 1$), thus change the strain in the MOS channel. This will ultimately degrade the device performance and must be avoided. So, instead of thermal oxidation at approximate 1100℃ as usual, low temperature oxidation is used in temperature range of 800~ 850℃. In our experiments the gate oxide thickness is 11nm, confirmed by C~ V measurements, which needs only very short oxidation time.

After gate polysilicon and source/drain implantation, the wafers are annealed for 15s at 960℃ in N_2 atmosphere.

4　Results and discussion

After MBE-grown structures are completed, the sample is tested by atomic force microscope (AFM) and double crystal X-ray diffraction (DCXRD). Results shown in Fig. 4 indicate the RMS is 1.02nm in a scanning rang of 25μm × 25μm. Figure 4(b) is the enlarged picture of Fig. 4 (a) with scanning range of 5μm×5μm. DCXRD result is shown in Fig. 5. The position of SiGe peak and the extended width of half maximum (FWHM) of X-ray diffraction peaks indicate that relaxed SiGe layer is attained.

Figure 6 shows the $I_{leakage}$ current of strained Si heterojunction PMOSFET at V_{gs}= 0V. The leakage current density is 135pA/μm (@V_{ds}= − 5V), measured by HP Agilent 4155B.

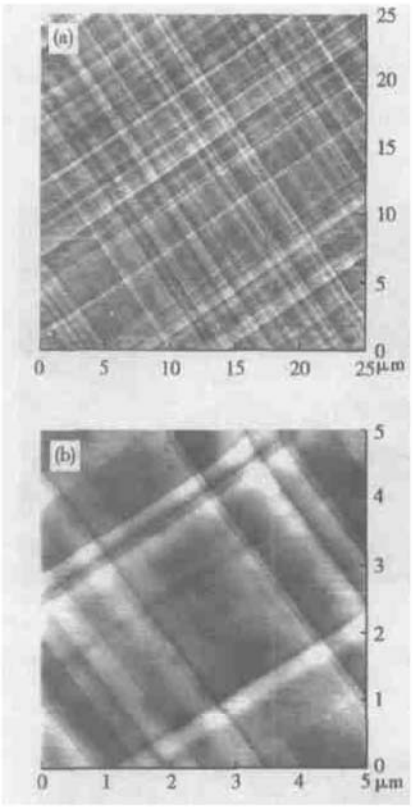

Fig. 4　AFM tests of samples(RMS= 1.02nm)

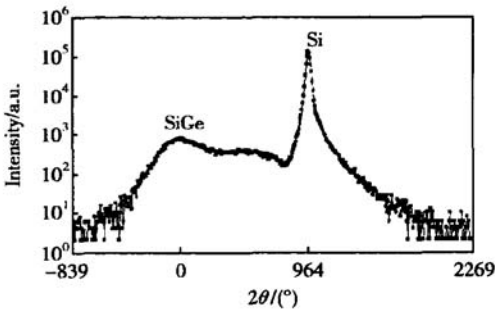

Fig. 5　X-ray (004) rocking curves of samples

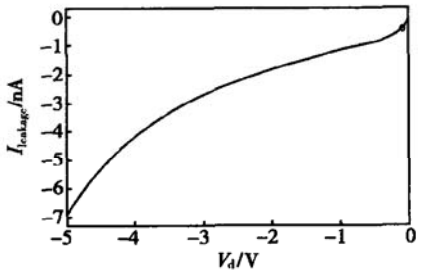

Fig. 6　$I_{leakage}$ versus V_d at V_g= 0V

Figure 7 to Figure 10 show the output I~ V characteristics of strained Si heterojunction pMOS-

FETs and that of bulk-Si pMOSFETs processed similarly, which prove obvious improvements of device performance using low-temperature (LT) Si technology. The sweep voltage applied on both gate electrodes is 0~ 10V. From the experimental results, it is found that I_d curve in strained Si pMOSFET is flatter than that in bulk-Si pMOSFET, which means the output impedance r_0 is larger. This conclusion is now under investigation, which is likely due to the different layer structures of strain-Si pMOSFET and channel doping. This is advantageous for analog IC design such as analog amplifiers due to higher intrinsic gain ($g_m r_0$). For low channel doping concentration ($1\times10^{16}cm^{-3}$), V_T of strain-Si pMOSFET extracted from Fig. 8 is -0.4V, while that of Si pMOSFET extracted from Fig. 9 is -1.2V due to the absence of channel doping adjustment.

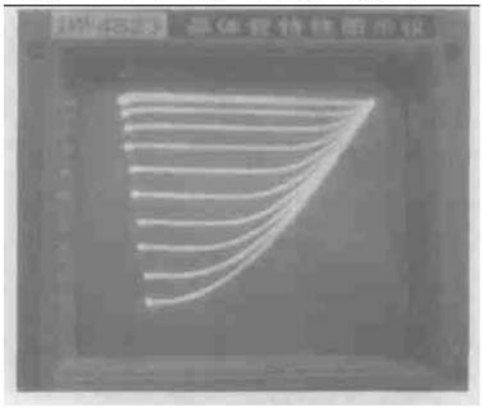

Fig. 7 Output I-V characteristics of strained Si pMOSFET (x-coordinate: 1V/div; y-coordinate: 1mA/div)

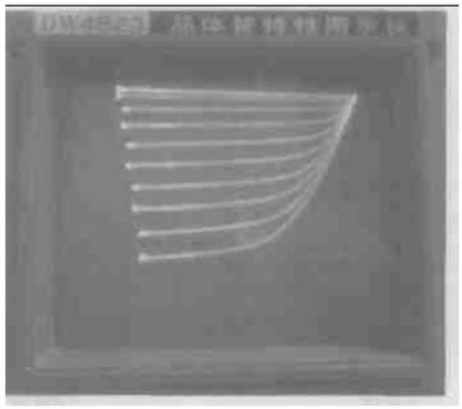

Fig. 8 Output I-V characteristics of bulk Si pMOSFET (x-coordinate: 2V/div; y-coordinate: 1mA/div)

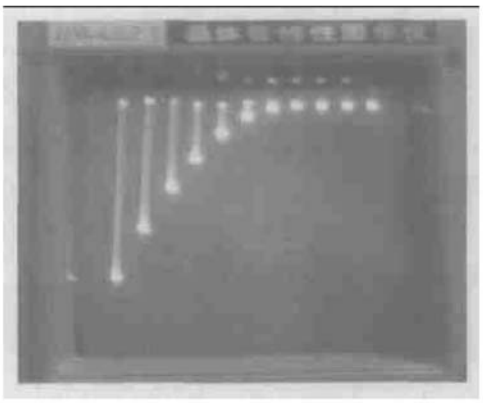

Fig. 9 I_{ds} versus V_{gs} characteristics of strain Si pMOSFET (x-coordinate: 0.1V/div; y-coordinate: 10μA/div)

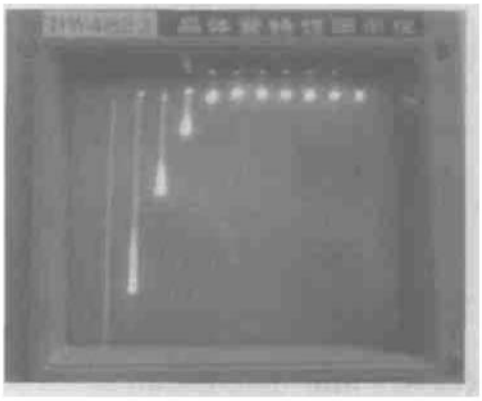

Fig. 10 I_{ds} versus V_{gs} characteristics of bulk-Si pMOSFET (x-coordinate: 0.2V/div; y-coordinate: 10μA/div)

Using the following formulations,

$$I_{ds} = -\frac{1}{2}(W/L)\mu_p C_{ox}(V_{gs} - V_{th})^2$$

$$G_m = \frac{\Delta I_{ds}}{\Delta V_{gs}}$$

$$\frac{\mu_{p,ss}}{\mu_{p,si}} = \frac{I_{ds,ss}(V_{gs,si} - V_{th,si})^2}{I_{ds,si}(V_{gs,ss} - V_{th,ss})^2}$$

where $\mu_{p,ss}$ and $\mu_{p,si}$ refer to the hole mobility of strained Si and bulk Si, respectively, the induced saturate transconductance G_m and mobility enhancement $\mu_{p,ss}/\mu_{p,si}$ vs V_{gs} are shown in Fig. 11 and Fig. 12.

In Fig. 11, $G_{m,ss}$ and $G_{m,si}$ refer to the transconductance of strained Si and bulk Si pMOSFET, re-

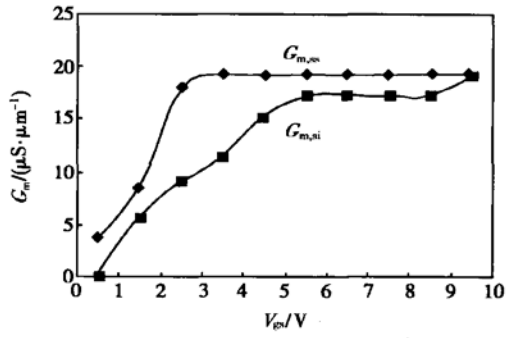

Fig. 11　G_m versus V_{gs} at 300K with $W/L = 52\mu m/4.5\mu m$

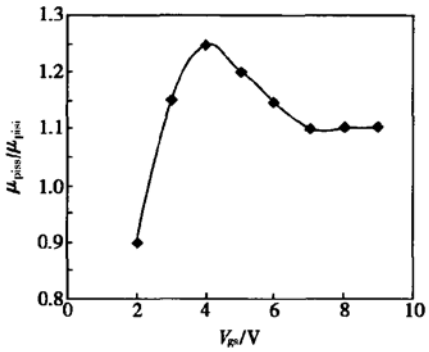

Fig. 12　Enhancement of the hole saturation mobility at 300K

spectively. In a wide range of V_{gs}, $G_{m,ss}$ maintains constant, with maximum amplitude twice times higher than that of $G_{m,si}$ at V_{gs}= 3V. From Fig. 12, when V_{gs} is close to 3.5~ 4V, 25% of the maximum mobility enhancement can be achieved. Unfortunately, it is also found when V_{gs} is below 2V, the hole mobility is degraded. For lower V_{gs}, the holes in strain-Si pMOSFET are confined near Si/SiGe hetero interface. Due to alloy scattering brought by Ge component and still higher threading dislocations (TD) density compared to that of Si pMOSFET, hole mobility is decreased relatively. Details of the reasons are still under investigation.

5 Conclusion

In this paper, fabrication of strained Si channel heterojunction pMOSFETs with LT-Si technology is introduced, with standard Si processes except for gate oxidation and annealing due to temperature limitations.

The thickness of relaxed $Si_{0.8}Ge_{0.2}$ epitaxy layer is reduced to less than 400nm with RMS of the strained Si surface less than 1.02nm. Device measurements indicate that hole mobility has been enhanced by a maximum factor of 1.25.

Refer to the experimental results achieved by Fitzgerald et al. from MIT[8], higher Ge fraction in relaxed SiGe layer results in higher hole mobility enhancement compared to that of the bulk Si MOSFETs processed similarly.

Acknowledgement　The authors would like to acknowledge discussions with Prof Harold Gamble from Northern Ireland Semiconductor Research Centre and X-ray rocking curve measurement aid from Institute of Physics and Center for Condensed Matter Physics, The Chinese Academy of Sciences.

References

[1] Rim K, Hoyt J L, Gibbons J F. Fabrication and analysis of deep submicron strained-Si n-MOSFET's. IEEE Trans Electron Devices, 2000, 47(7): 1406

[2] Bernard S. Meyerson. UHV/CVD Growth of Si and Si∶Ge alloys: chemistry, physics, and device application. Proceeding of the IEEE, 1992, 80(10): 1592

[3] Shi Jin, Huang Wentao, Chen Peiyi. Strained Si-channel heterojunction n-MOSFET. Chinese Journal of Semiconductors, 2002, 23(7): 685

[4] Li Chen, Luo Guangli, Liu Zhinong, et al. Novel strained Si/relaxed SiGe channel PMOSFETs. Thin Solid Films, 2002, 409(1): 112

[5] Chen H, Guo L W, Cui Q, et al. Low temperature buffer layer for growth of a low-dislocation-density SiGe layer on Si by molecular-beam epitaxy. J Appl Phys, 1996, 79: 1167

[6] Rosenbald C, Stangl J, Müller E, et al. Strain relaxation of graded SiGe buffers grown at very high rates. Materials Science and Engineering B, 2000, 71: 20

[7] Holländer B, Lenk St, Mantl S, et al. Strain relaxation of pseudomophic $Si_{1-x}Ge_x$/Si(100) heterostructures after hydrogen or helium ion implantation for virtual substrate fabrication. Nuclear Instruments and Methods in Physics Research B, 2001, 175-177: 357

[8] Fitzgerald E A, Lee M L, Leitz C W, et al. MOSFET channel

engineering using stratined Si, SiGe, and Ge channel. ECS Meeting Proceedings, Paris, 2003

应用 400℃低温 Si 技术制备应变 Si 沟道 pMOSFET*

梅丁蕾[1] 杨谟华[1] 李竞春[1] 于 奇[1] 张 静[2] 徐婉静[2] 谭开洲[2]

(1 电子科技大学微电子与固体电子学院, 成都 610054)
(2 模拟集成电路国家重点实验室, 重庆 400060)

摘要: 在利用分子束外延方法制备 SiGe pMOSFET 中引入了低温 Si 技术. 通过在 Si 缓冲层和 SiGe 层之间加入低温 Si 层, 提高了 SiGe 层的弛豫度. 当 Ge 主分为 20% 时, 利用低温 Si 技术生长的弛豫 $Si_{1-x}Ge_x$ 层的厚度由 UHVCVD 制备所需的数微米降至 400nm 以内, AFM 测试表明其表面均方粗糙度(RMS) 小于 1.02nm. 器件测试表明, 与相同制备过程的体硅 pMOSFET 相比, 空穴迁移率最大提高了 25%.

关键词: 锗硅; 低温硅; 弛豫; 线位错

EEACC: 2560R

中图分类号: TN386 **文献标识码**: A **文章编号**: 0253-4177(2004) 10-1221-06

* 模拟集成电路国家重点实验室基金资助项目(合同号: 2000JS09.3.1.DZ02)
梅丁蕾 男, 1981 年出生, 硕士研究生, 研究方向为 SiGe CMOS 器件与电路.
2003-12-25 收到, 2004-05-08 定稿