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Design Guideline of Ultra Thin Body MOSFET*

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Abstract: Simulation method is used to provide a guideline for ultra thin body(UTB) MOSFET designs. Three important parameters of the UTB MOSFET, i. e. the raised S/D height, Ge mole fraction of the Ge_xSi_{1-x} gate, and the silicon body thickness, are comprehensively analyzed and optimized. The optimal region of feasible Ge mole fraction and the silicon body thickness for low operating power device are given. As the simulation results show that through changing Ge mole fraction coupled with the silicon body thickness tuning, UTB device with good performance can be obtained.

Key words: ultra thin body MOSFET; raised S/D height; Ge mole fraction; silicon body thickness
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1 Introduction

Ultra thin body (UTB) MOSFET, which combines the best features of bulk CMOS (e. g., deep source/drain regions) with those of SOI (e. g., ultra-thin channel and dielectric insolating layer), is considered as the promising structure for ultimate device[1~3]. There are many literatures related with UTB MOSFET, yet, most focus on the experimental research which only gives some results on a special structure without pointing out what kind of device parameters are optimal. Until now, there is still no analytical model that can clearly describe the operation mechanism of UTB MOSFET, especially for the mechanisms of coupling effect between the front and back interfaces and the channel quantization effect. Moreover, for different performance requirement, the choice of device parameters is very important due to the tradeoffs among the device parameters. In order to reduce some negative effects caused by the ultra thin body, such as strong coupling effect between the front and back interfaces and channel quantization effect, optimizations on different aspects of geometric parameters and physical parameters of UTB structure are amply necessary, especially for nano-scale UTB applications[4,5].

In most reported UTB structures, the p^+ doped Ge_xSi_{1-x} which is fairly compatible to the standard Si CMOS process is used as the gate material in order to maintain the positive threshold voltage[6]. Ge_xSi_{1-x} is adopted as a gate material also because the work function can be easily adjusted with changing Ge mole fraction[7,8]. However, when the workfunction is being adjusted, some negative

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effects will appear as shown in our simulation results and optimal Ge mole fraction range should be found. In addition, in UTB MOSFET, there is another key dimensional parameter, i. e., thickness of silicon body. Simulation results show that the thickness of the silicon body has a significant effect on the device performance. But what kind of thickness should be used under specific channel length is still an unanswered question as far as the knowledge of the authors. Finding an optimal range of the body thickness for different feature size of UTB, especially the combinations of optimal silicon body thickness and optimal range of Ge mole fraction, is what we have done in this paper. According to International Technology Roadmap for Semiconductors (ITRS) criterion for low operating power (LOP) device, we focus our attention on optimizing three important parameters of the UTB MOSFET with Ge_xSi_{1-x} gate. For the first time, the optimized range of Ge mole fraction and the silicon body thickness is given for the LOP device. Our simulation results show that a significant improvement of the MOSFET performance can be achieved, without any degradation of the short-channel performance or sacrifice on "on-state and off-state" behavior of the devices, by careful tuning of the Ge mole fraction and the silicon body thickness.

2 Simulation structure

Simulations are performed with a two-dimensional (2D) device simulator-ISE 8.0. The schematic cross section view of the simulated structure is shown in Fig. 1. The gate length of the simulated UTB MOSFET is 50nm with 2nm gate oxide. Correspondingly, a light and uniform body doping ($10^{15}cm^{-3}$) is adopted. The doping concentrations for LDD region and source/drain region are fixed to $5\times10^{19}cm^{-3}$ and $10^{20}cm^{-3}$, respectively. The height of the Ge_xSi_{1-x} gate and the silicon oxide sidewall is 150nm. The buried oxide is 100nm. Moreover, the S/D electrodes are at the side of the S/D region. In this paper, we optimized three important parameters of the UTB device, they are, height of the raised S/D (t_{SD}), Ge mole fraction (x), and the silicon body thickness (t_{Si}). As conducting the optimization, we use ITRS specification for LOP application, which determines what kind of value ranges of these three parameters is optimal, i. e., $I_{on}>600\mu A/\mu m$, $I_{off}<300pA/\mu m$, and $\Delta V_{T\_DIBL}/V_T<0.3$ as the criterion.

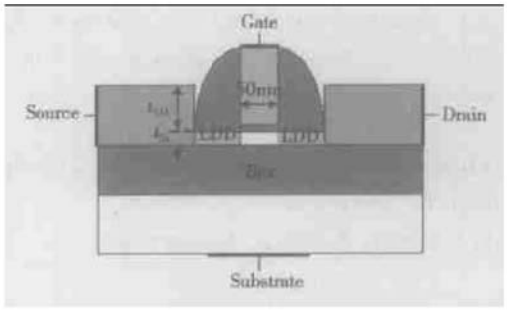

Fig. 1 Schematic cross section view of the simulated UTB MOSFET

3 Results and discussion

3.1 Impact of variable raised S/D height on the device current

Due to the S/D series resistance, many reported UTB MOSFETs obtain very small on-state current. Obviously, this S/D series resistance is a bottleneck when further improvement on UTB device performance is wanted. In order to reduce the negative impact of the S/D series resistance on the device on-state current, S/D elevation technique should be used in UTB device. Figures 2 and 3 show the effect of different raised S/D height on the on-state and off-state current with increasing silicon body thickness when Ge mole fraction equals to 0 or 1. It can be seen that the raised S/D height has a trivial influence on the off-state current of the device, and the reason is that the off-state current is the pn junction leakage between S/D and the channel. When the raised S/D height increases, it has no influence on the pn junction, thus, the off-state current is unchanged. However,

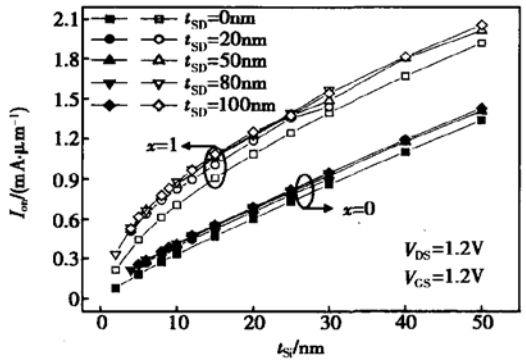

Fig. 2　Effect of the raised S/D height on the on-state current of UTB MOSFET @ V_{GS}= 1.2V, V_{DS} = 1.2V and Ge mole fraction equals to 0 or 1

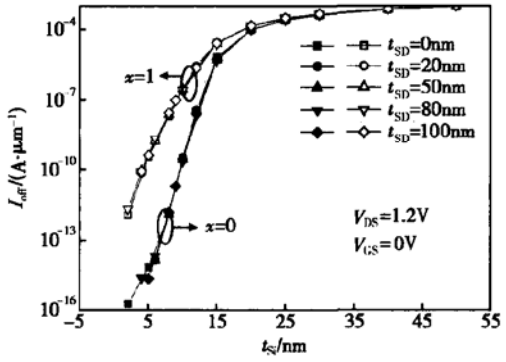

Fig. 3　Effect of the raised S/D height on the off-state current of UTB MOSFET @ V_{GS}= 0V, V_{DS}= 1.2V and Ge mole fraction equals to 0 or 1

the raised S/D height has an observable impact on the on-state current. This is because at on-state the cross area of the S/D will increase with the increasing of raised S/D height. This will lead to reduce S/D extended resistance which is one part of the S/D series resistance, resulting in enhanced on-state current. But as the raised S/D height continuously increases, the influence of the extended resistance becomes smaller, thus the on-state current will increase very little. As our simulation results show, when the raised S/D height is over 100nm, the on-state and off-state currents of the device will not change. So in following simulation, in order to neutralize the influence of the raised S/D height, we adopt 100nm as the default value for raised S/D height. Figures 2 and 3 also illustrate the effects of Ge mole fraction on the on-state current and off-state current. A more detailed analysis is given in subsection 3.2.

3.2　Optimization of Ge mole fraction and silicon body thickness

Ge mole fraction and the silicon body thickness are two important parameters in UTB MOSFET. The threshold voltage can be adjusted by changing Ge mole fraction and the current path from source to drain can be controlled by the silicon body thickness. The simulation results show that if an optimal Ge mole fraction is combined with an optimal silicon body thickness, good performance can be obtained. Figure 4 shows the V_T rolling-off caused by DIBL effect with different Ge

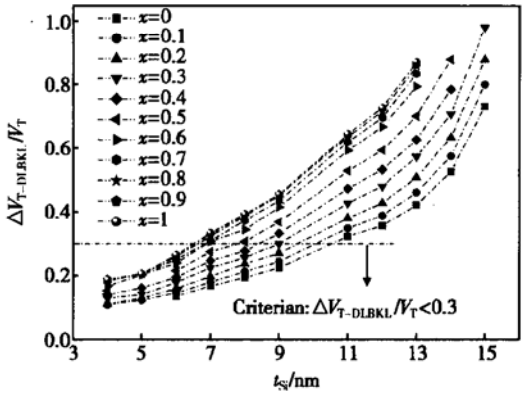

Fig. 4　Impact of Ge mole fraction and the silicon body thickness on DIBL effect, where ΔV_{T_DIBL} = $V_T(V_{DS}$= 0.05V) − $V_T(V_{DS}$= 1.2V)

mole fraction and different silicon body thickness. The dash-dot line marks our optimization criterion, i. e., $\Delta V_{T\_DIBL}/V_T < 0.3$, where V_T is the gate voltage @ $I_{ds}= \frac{W}{L}\times 5\times 10^{-7}$A/μm and V_{DS}= 0.05, and $\Delta V_{T\_DIBL}= V_T(V_{DS}= 0.05V) - V_T(V_{DS}= 1.2V)$. With decreasing silicon body thickness, the number of electric lines from drain to source is also reduced, thus the influence of drain voltage on source barrier is minimized. So the reduction of silicon body thickness can efficiently suppress DIBL effect. In addition, if we do not change the silicon body thickness, and only increase the Ge mole frac-

tion, enhancement of the ratio $\Delta V_{T\_DIBL}/V_T$ can be observed. For example, with 12nm silicon body thickness, $\Delta V_{T\_DIBL}/V_T$ in the device, with Ge mole fraction being equal to 0, is 0.355. However, it is 0.726 with Ge mole fraction being equal to 1. This is because that the barrier will decrease when the Ge mole fraction is increased, which has been shown in Fig. 5. From Fig. 5, we can see that when the drain voltage increases from 0.05 to 1.2V, the reduction of the channel potential is 0.0697V with Ge mole fraction being equal to 0, while the reduction is 0.1347V with Ge mole fraction being equal to 1. That is to say, with the increasing of Ge mole fraction, the decrement of the barrier is increased, which results in the enhancement of V_T rolling-off.

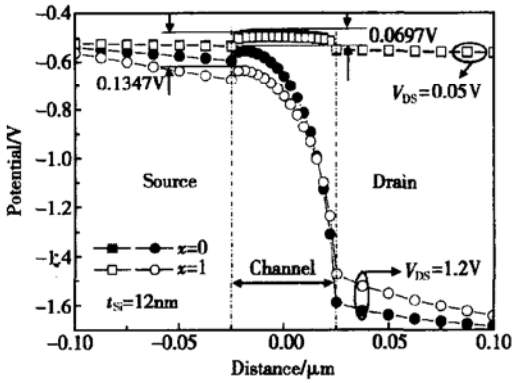

Fig. 5 Comparison of potential distribution along the channel with increased drain voltage, where Ge mole fraction equals to 0 or 1

Figures 6 and 7 show the on-state and off-state current of the device with different Ge mole fraction and the silicon body thickness, the dash-dot line marks the LOP ITRS criterion. As the silicon body thickness is reduced, some part of the current path from source to drain is eliminated. The electron density is also greatly affected by changing the thickness of silicon body. Figure 8 compares the electron density in the channel region at V_{GS}= 0, V_{DS}= 1.2V under different silicon body thicknesses. From Fig. 8 it can be seen that the electron density of UTB device with 4nm silicon body thickness is much smaller than that of UTB device with 12nm silicon body thickness. And this

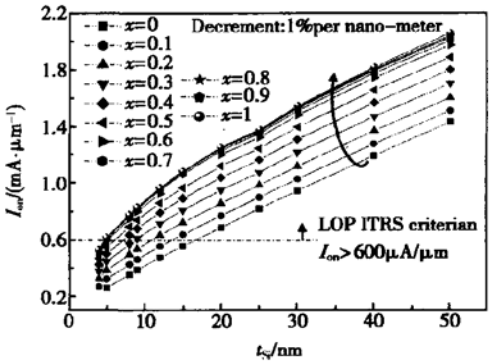

Fig. 6 Impact of Ge mole fraction and the silicon body thickness on the on-state current of the device

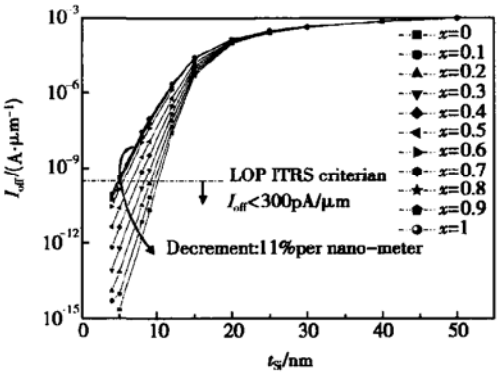

Fig. 7 Impact of Ge mole fraction and the silicon body thickness on the off-state current of the device

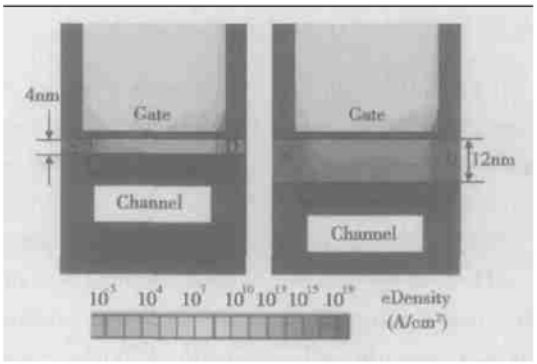

Fig. 8 Electron density of the channel region with 4nm and 12nm silicon body thickness at V_{GS}= 0V, V_{DS}= 1.2V

phenomenon definitely explains the current reduction as shown in Figs. 6 and 7. From Figs. 6 and 7, significant decreasing of on-state and off-state current is observed with decreasing silicon body thickness. But the current reduction extent is different

for on-state and off-state. At on-state, although some parts of the current path are eliminated with decreasing silicon body thickness, the electron mobility enhancement due to the channel being lightly doped can make up the negative effect. In Fig. 6, if the silicon body thickness reduces by 1nm, the on-state current will reduce by 1%. While at off-state, the current path is the main factor to determine the value of the off-state current. So, in Fig. 7 the current decrement is 11% per nano-meter decrement of the thickness. For example, with the silicon body thickness decreasing from 9nm to 8nm, the on-state current reduces from 3.8×10^{-4}A/μm to 3.5×10^{-4}A/μm, while the off-state current is 1.9×10^{-11}A/μm to 1.5×10^{-12}A/μm, respectively. In summary, decreasing the silicon body thickness is a very effective way to increase the ratio of the on-state and off-state current and get better performance device.

From above analysis, there is a matching problem between Ge mole fraction and silicon body thickness just as shown in Figs. 4~ 8. According to the optimization criterion, the optimization region of the feasible Ge mole fraction and the feasible silicon body thickness of UTB MOSFET can be obtained, just as shown in Fig. 9. The shadow region is the design window for UTB MOSFET. From Fig. 9 we can see that the optimal Ge mole fraction is varied from 0.35 to 1 and correspondingly the optimal silicon body thickness is varied from 4.75nm to 8.25nm. For a given Ge mole fraction

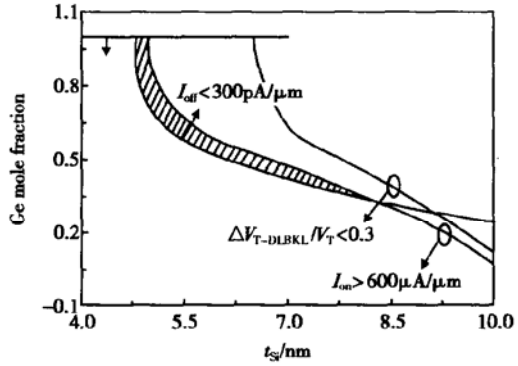

Fig. 9　Region of the feasible Ge mole fraction and the feasible silicon body thickness of UTB device

(e.g. 0.5), the allowable range of the silicon body thickness for ITRS specification can be chosen (e.g. 6~ 7nm) in the shadow region, and for a given silicon body thickness (e.g. 6nm), there is also a feasible range (e.g. 0.5~ 0.6) for Ge mole fraction to be chosen. In both cases, the device performance with the selected parameters from the optimal window will meet the ITRS specification for LOP device. Figure 10 is the output characteristic comparison between the UTB MOSFET reported in Ref. [8] and our optimized UTB MOSFET. It can be seen that the on-state current of the optimized

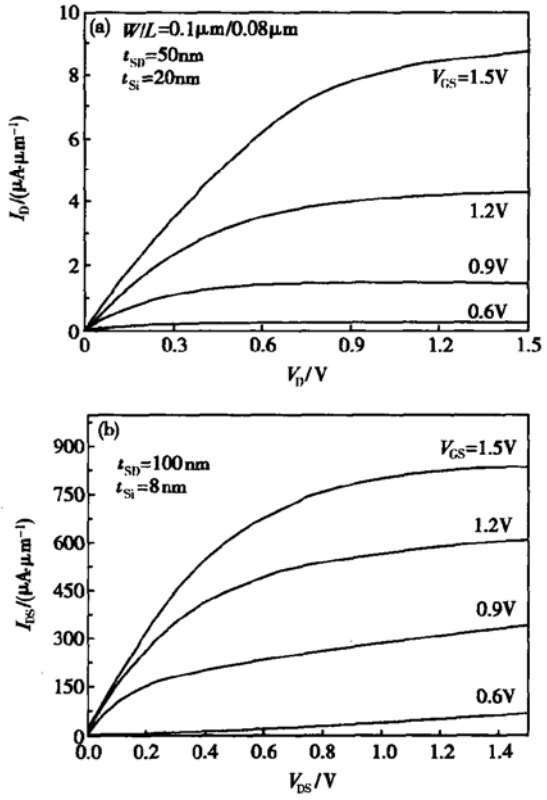

Fig. 10　Output characteristic comparison between UTB MOSFET reported in Ref. [8] (a) and optimized UTB MOSFET (b)

UTB MOSFET is about 800μA/μm, which is nearly 100 times of that reported UTB MOSFET. Strong evidences show that better performance device which satisfies the ITRS LOP specification can be obtained, without any degradation of the short-channel performance or sacrifice of "on-state" and

"off-state" behavior of the device, by careful tuning of the Ge mole fraction and the silicon body thickness.

4 Conclusion

Optimization of the three important parameters of UTB MOSFET, i.e. the raised S/D height, Ge mole fraction, and silicon body thickness, is carried out in this paper. Simulation results show that for gate length of 50nm UTB MOSFET, when the raised S/D height is over 100nm, the on-state and off-state current of the device will not change with the increasing raised S/D height. For the first time, the optimal region of Ge mole fraction and the silicon body thickness is given according to ITRS criterion for LOP device. Without any degradation of short-channel performance or sacrifice on "on-state" and "off-state" behavior of the device, a significant improvement of the MOSFET performance can be obtained by careful tuning of the Ge mole fraction and the silicon body thickness. It will be a very useful guideline of the nano-meter UTB MOSFET design.

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超薄体 MOSFET 的结构优化*

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摘要: 对 UTB 器件的各结构参数进行了优化, 给出了 UTB 器件设计的指导方向. 在 UTB 器件的设计中, 有三个重要参数, 即器件的源漏提升高度、锗硅栅(Ge_xSi_{1-x})中 Ge 含量的摩尔百分比和硅膜的厚度, 并对这三个结构参数对器件性能的影响进行了模拟分析, 给出了器件各结构参数的优化方向, 找出了可行 Ge 含量的摩尔百分比和可行硅膜厚度之间的设计容区. 通过模拟分析发现, 只要合理选择器件的结构参数, 就能得到性能优良的 UTB 器件.

关键词: 超薄体 MOSFET; 提升源漏高度; Ge 摩尔百分比; 硅膜厚度;

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