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A 30 Finger Microwave Power SiGe HBT with 23V BV_{CBO} and f_T 7GHz*

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Abstract: With modified necessary steps for SiGe implementation, multi-finger power SiGe HBT devices are fabricated in a CMOS process line with 125mm wafer. The devices show quite high BV_{CBO} 23V. The current gain is very stable over a wide I_C. The f_T is up to 7GHz at a DC bias of I_C= 40mA and V_{CE}= 8V, which show high current handling capability. Under continuous conditions in B operation, the 31dBm output power, 10dB G_p, and 33.3% of PAE are obtained at 3GHz. Based on extensive tests, it has been demonstrated that the yield on a wafer is up to 85%, which means that the research results are capable of commercialization.

Key words: SiGe HBT; f_T; power
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1 Introduction

Because of high current handling capability per unit area along with high voltage operation, bipolar transistors in particular have been investigated. Although silicon bipolar transistors have been demonstrated with high power levels at low frequencies, the RF power, efficiency and gain of the silicon BJTs deteriorate as the frequency increases. Consequently, a new contender for Si-based RF and microware circuit applications is needed. GaAs HBTs have shown good efficiency and power gain at high frequency, but cost and level-of-integration make GaAs HBTs less attractive in widespread usage. SiGe HBT is competitive with GaAs HBT with the processing maturity, integration levels, yield, and cost. With the mature Si process technology, the SiGe HBT microwave monolithic integrated circuits (MMIC′s) have received great attention as a potential candidate for wireless communication market. Recent advances in the growth of SiGe epitaxial layers have led to high quality SiGe heterojunctions and consequently high performance SiGe HBTs[1,2]. Nevertheless, such impressive results are generally obtained at the expense of a considerable increase in process complexity. At the same time, the device with high f_T but low power is not useful enough for MMIC′s, in which implement of high performance SiGe power devices will be the key to the success of realizing a microwave system on a chip using Si substrate. A high collector-base breakdown voltage, BV_{CBO}, is generally desired to achieve high output power. This requirement leads to a much thicker collector than for small-signal transistors, which in turn lim-

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its the operating frequency since the cut-off frequency is now dominated by collector transit delay time. Thus, it is challenging to achieve high BV_{CBO} and high f_T simultaneously.

In this paper, we describe a quite simple technology to SiGe HBT fabrication, in which only 6 patterns are needed. Using the double-mesa technology, a multi-finger (30 fingers) power SiGe HBT with high BV_{CBO} 23V and high f_T 7GHz is developed. For a 60-finger SiGe HBT, under continuous conditions, at 3GHz, the 31dBm output power, 10dB G_P, and 33.3% of PAE are obtained.

2 SiGe HBT structure and process of fabrication

The devices were fabricated in a normal CMOS process line. Figure 1 shows a schematic cross-section of the investigated SiGe HBT.

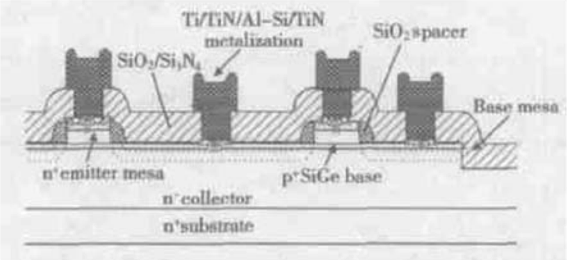

Fig. 1 Schematic cross-section of the investigated SiGe HBT

Arsenic doped n^+ ($\rho = 0.003\Omega \cdot cm$) Si(100) wafers were used as the substrate. After an atmospheric pressure epitaxial n^- ($\rho = 0.2\Omega \cdot cm$) layer was grown on the substrate, a self-made ultra-high vacuum chemical vapor deposition (UHVCVD) setup in Tsinghua University was used for epitaxial growth of SiGe base. The details of UHVCVD system were described elsewhere[3,4]. The epitaxial growth was carried out at 580℃. The base profile consisted of four layers: 10nm undoped buffer Si layer, 40nm B-doped ($4 \times 10^{18} cm^{-3}$) $Si_{0.87}Ge_{0.13}$, 10nm undoped $Si_{0.87}Ge_{0.13}$, and 20nm undoped Si cap layer. The detailed growth process was depicted in Refs. [5, 6]. The fabrication started with poly-Si deposition and P^+ implantation. After the base mesa was formed by RIE technology, an oxidation layer was formed by LPCVD, which served as a hard mask for preventing B^+ dopants from entering n-type emitter mesa. Except being used as a mask, this oxidation layer also acts as a protecting layer of the B-C junction. Noticeably, this oxidation layer is crucial for preventing B-C leakage current, which was deposed as soon as the B-C junction was exposed. Then emitter mesas were formed by RIE technology. To keep the emitter from directly contacting the extrinsic base, sidewall SiO_2 spacers were formed. The thickness of sidewall was the trade-off between R_b and B-E junction leakage current. After extrinsic base contact implantation, the oxidation on emitter mesas was etched. TEOS and Si_3N_4 were deposited, patterned, and opened by dry etching and wet etching for contact hole formation on top of the emitter mesas and base mesa. The double dielectrics of the hole and the two-step etching process were crucial for preventing B-E leakage current and greatly improved the yield. Rapid thermal annealing is then performed at 880℃ for 20s for dopant diffusion and activation. The metallization consisted of a thin layer of Ti/TiN for low contact resistance, a sputtered Al-Si and TiN layer, which was an anti-reflecting layer. Following the passivation with PECVD Si_3N_4 and SiO_2, the process was completed by a 30min of heat treatment at 430℃ in N_2 ambient for alloying the metal/semiconductor contact.

3 Results and discussion

In order to obtain big current handling capability, multiple finger design for emitters and base-contacts was chosen. Figure 2 shows a SEM of a completed transistor, demonstrating good control of the overall manufacture process. The DC characteristics of the devices have been measured with Kathley4200 semiconductor parameter analyzer. Hard breakdown at 23V with very low leakage current $I_{CBO} < 10nA$ at $V_{CB} = 20V$ was obtained for the reverse biased B-C junction with an open emitter configuration, which was governed by the doping concentration $2\times10^{16}\mathrm{cm}^{-3}$ and the thickness $2\mu\mathrm{m}$ of the n^{-} epi-layer. This is an indication for a good quality of epi-layer growth, i. e. no dislocations were generated at the substrate-epi-layer interface and in the SiGe layer during the thermal processing. The I-V characteristic of a 30-finger device is shown in Fig. 3 and the current gain is very stable over a wide I_{C}. The Gummel plot of the same HBT is shown in Fig. 4. The collector current I_{C} exhibits an almost ideal behavior over a big V_{BE}.

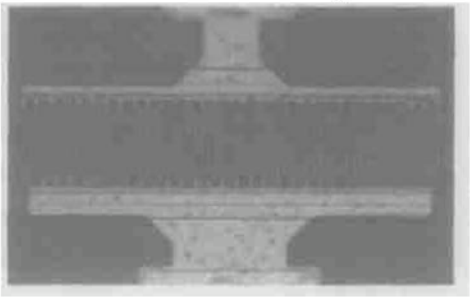

Fig. 2 SEM for a $30\times1.6\mu\mathrm{m}\times30\mu\mathrm{m}$ SiGe HBT

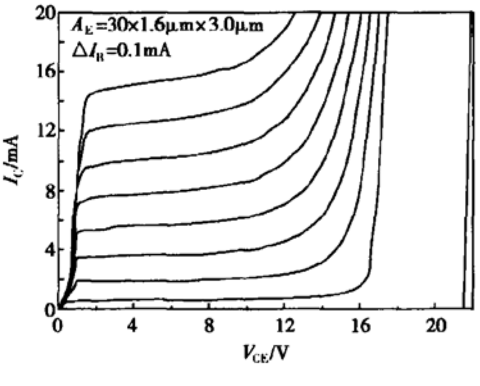

Fig. 3 I-V characteristics for a $30\times1.6\mu\mathrm{m}\times30\mu\mathrm{m}$ SiGe HBT

It is well known that the major advantage of using heterojunction as the E-B junction of a SiGe HBT is to enhance the current gain (β) of the transistor for fixed bias. For identical constructed devices, the ratio of β between SiGe HBT and Si BJT can be given by[7]

$$\left.\frac{\beta_{\mathrm{SiGe}}}{\beta_{\mathrm{Si}}}\right|_{V_{\mathrm{BE}}}\approx\left.\frac{J_{\mathrm{C,SiGe}}}{J_{\mathrm{C,Si}}}\right|_{V_{\mathrm{BE}}}\approx\frac{\bar{\gamma}\bar{\eta}\times\frac{\Delta E_{\mathrm{g,Ge}}(\mathrm{grade})}{kT}\times\mathrm{e}^{\Delta E_{\mathrm{g,Ge}}(0)/kT}}{1-\mathrm{e}^{-\Delta E_{\mathrm{g,Ge}}(\mathrm{grade})/kT}} \tag{1}$$

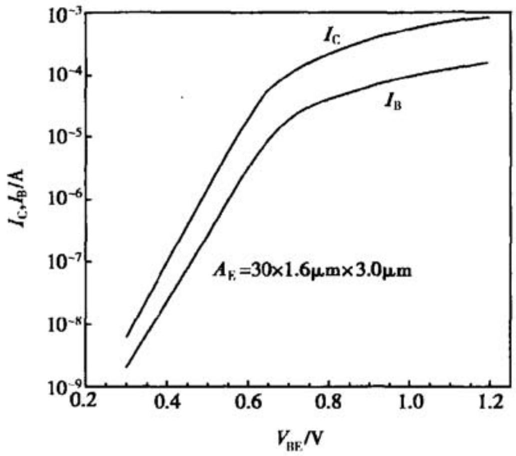

Fig. 4 Gummel plot for a $30\times1.6\mu\mathrm{m}\times30\mu\mathrm{m}$ SiGe HBT

Associated with Ref. [8], for SiGe HBT with polysilicon emitter, the current gain is given to a good approximation by

$$\beta=\frac{n_{0\mathrm{B}}}{p_{0\mathrm{E}}}\times\frac{D_{\mathrm{nB}}}{D_{\mathrm{p}2}}\times\left(\frac{w_{\mathrm{E}}}{w_{\mathrm{B}}}+\frac{D_{\mathrm{p}2}L_{\mathrm{p}1}}{w_{\mathrm{B}}D_{\mathrm{p}1}}\tanh\frac{w_{1}}{L_{\mathrm{p}1}}\right)\times\exp(\Delta E_{\mathrm{g}}/kT) \tag{2}$$

Using expression (2), the β versus N_{B} is simulated. The boron doping level in SiGe base layer varies from $4\times10^{18}\mathrm{cm}^{-3}$ to $10^{19}\mathrm{cm}^{-3}$. And in the simulations, the SiGe is modeled using $\Delta E_{\mathrm{g}}=0.74x$ (x is the Ge composition). Figure 5 shows the β comparison between simulation results and measured values. The simulation fits well for all 5 devices. The incremental change in the boron doping level of different wafer is clearly reflected in the

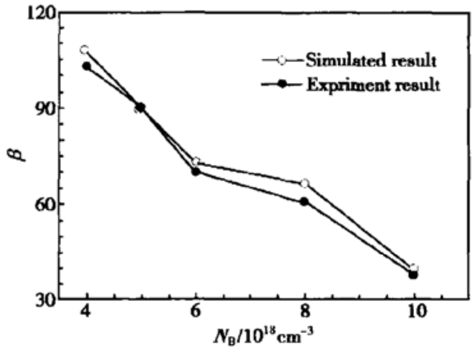

Fig. 5 β comparison between simulated values and measured values for N_{B} from $4\times10^{18}\mathrm{cm}^{-3}$ to $10^{19}\mathrm{cm}^{-3}$

mean current gain value. These results demonstrate good control of the concentration of epitaxial base. It provides the possibility for optimizing maximum oscillation frequency $f_{\max}$ and β by changing N_B.

S-parameter measurements have been performed, using HP8510 network analyzer, to evaluate the high frequency performances of this SiGe HBT process. For high current handling capability, 30 fingers are designed. Although emitter area is quite big as $30\times1.6\mu m\times30\mu m$, the device still has a high cutoff frequency 7GHz at a DC bias $I_C=$ 40mA and $V_{CE}=$ 8V, and the B-C junction breakdown voltage is up to 23V with collector thickness being designed as $2\mu m$. For higher BV_{CBO}, thicker collector thickness $3\mu m$ is designed and its BV_{CBO} is up to 40V. Figure 6 illustrates f_T characteristics of the device with $3\mu m$ collector. It can be seen that the transistor maintains a 4.2GHz f_T at $I_C=$ 40mA and $V_{CE}=$ 8V. The following expression can explain the reason of f_T decrease[9].

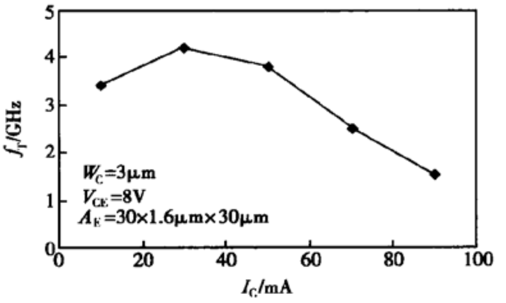

Fig. 6 f_T versus I_c, for a $30\times1.6\mu m\times30\mu m$ SiGe HBT at $V_{CE}=$ 8V

$$\frac{1}{2\pi f_T}=\tau_e+\frac{W_B^2}{\eta D_n}+\frac{X_C}{2v_{sat}}+\frac{C_{BE}+C_{BC}}{g_m}+R_C C_{BC} \tag{3}$$

where X_C is the collector depletion width and R_C is the series resistance of the collector. For higher BV_{CBO}, lower collector doping N_C and thicker collector are often designed, which increase X_C and R_C respectively. f_T thus decreases. With consideration of the dopant outdiffusion in the collector during atmospheric pressure epitaxy, BV_{CBO} and BV_{CEO} should be higher if n^- epi-layer was grown by low pressure epitaxy with the same thickness. Although it is difficult in achieving high f_T and high BV_{CEO} simultaneously, high $f_T BV_{CEO}$ value of 120GHz·V is still obtained.

For the power RF testing, a 60-finger SiGe HBT was connected in a common-base configuration with an external matching network. The device was tested in class B operation under continuous conditions. The DC bias on the output (collector) was 20V, and the RF input power was 21dBm. At 3GHz, the 31dBm output power, 10dB G_p, and 33.3% of PAE were obtained.

4 Conclusion

We have developed a 125mm 0.8μm SiGe HBT technology. This technology is characterized by simplicity and producibility. Despite the process is quite simple, excellent static and dynamic characteristics have been obtained, with BV_{CBO} 23V and f_T 7GHz. For a 60-finger SiGe HBT, at 3GHz, the 31dBm output power, 10dB G_p, and 33.3% of PAE were obtained.

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BV_{CBO}为23V且f_T为7GHz 30叉指微波功率SiGe HBT*

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摘要: 在125mm标准CMOS工艺线上, 对标准CMOS工艺经过一些必要的改动后, 研制出了多叉指功率SiGe HBT. 该器件的BV_{CBO}为23V. 在较大I_C范围内, 电流增益均非常稳定. 在直流工作点$I_C = 40$mA, $V_{CE} = 8$V测得f_T为7GHz, 表现出较大的电流处理能力. 在B类连续波条件下, 工作频率为3GHz时, 测得输出功率为31dBm, G_p为10dB, 且PAE为33.3%. 测试结果表明, 单片成品率达到了85%, 意味着该研究结果已达到产业化水平.

关键词: SiGe HBT; f_T; 功率管

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