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200Ms/s 177mW 8bit Folding and Interpolating CMOS A/D Converter*

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Abstract: A CMOS folding and interpolating analog-to-digital converter (ADC) for embedded application is described. The circuit is fully compatible with standard digital CMOS technology. A modified folding block implemented without resistor contributes to a small chip area. At the input stage, offset averaging reduces the input capacitance and the distributed track-and-hold circuits are proposed to improve signal-to-noise-plus-distortion ratio. The 200Ms/s 8bit ADC with 177mW total power consumption at 3.3V power supply is realized in standard digital 0.18μm 3.3V CMOS technology.

Key words: analog-to-digital converter; CMOS analog integrated circuits; folding and interpolating

EEACC: 1265H; 1280; 2570D

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1 Introduction

According to the development of SOC (system-on-chip) technique, many applications need an on-chip ADC as an analog/digital interface, such as Gigabit Ethernet[1], LCD driver[2], and hard disk channel drivers[3]. In these applications, minimum susceptibility to cross talk is of utmost important for an ADC, which is embedded in a noisy switching environment utilizing the same substrate as the digital components. A small chip area and power consumption of ADC is also a stringent requirement and no external trimming is allowed.

In the field of high speed ADC, the fastest ADC architecture reported to date is the flash-converter. However, an 8bit ADC based on a flash-type will require 256 very accurate and fast comparators, which consume a large chip area and power dissipation. Among various ADC architectures, the folding/interpolating technique is one of the candidates to overcome those drawbacks of the flash type ADC, and furthermore it is fully compatible with standard digital CMOS technology. In this converter, offset averaging technique is used to reduce the input capacitance[4] and the distributed track-and-hold circuits to improve SNDR[5,6]. A modified folding processor with MOS transistors replacing the conventional resistor load makes the design of following analog circuits easier. As a result, this ADC has a small chip area and power dissipation 177mW at conversion rate of 200MHz.

In this paper, the ADC with general folding/interpolating architecture is introduced. The proposed ADC and the detailed implementation are de-

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scribed.

2 Conventional folding and interpolating ADC

Figure 1 shows the conventional architecture of an 8bit folding and interpolating ADC, including two parts. The coarse ADC uses a flash-type architecture, while the folding/interpolating circuit which can reduce drastically the number of comparators and preamplifiers is designed in the fine ADC. A pre-amplifier array is placed proceeding to the folder. Distributed sample-and-hold circuit is combined with the pre-amplifier array[6]. The array of preamplifiers measures the difference between the input signal and the tap voltages generated by a resistive ladder. After resistor interpolats block whose interpolating factor is 8, 32 outputs are sent to the comparator array.

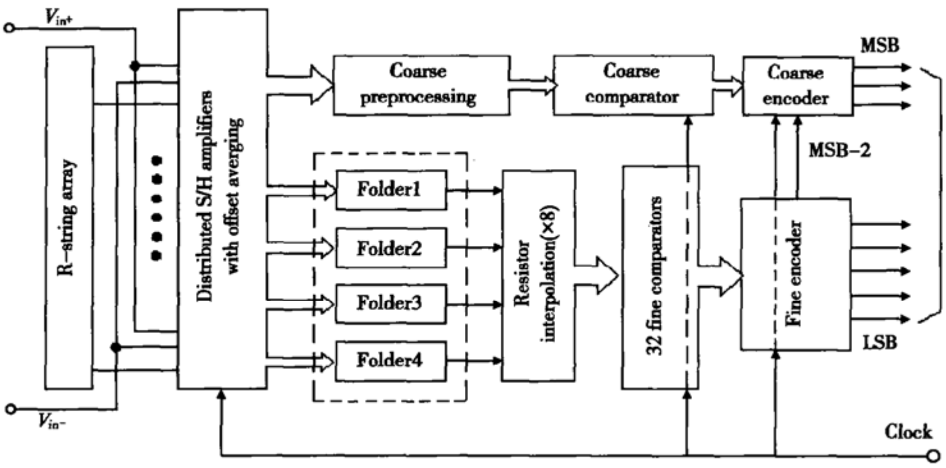

Fig. 1 Block diagram of the conventional

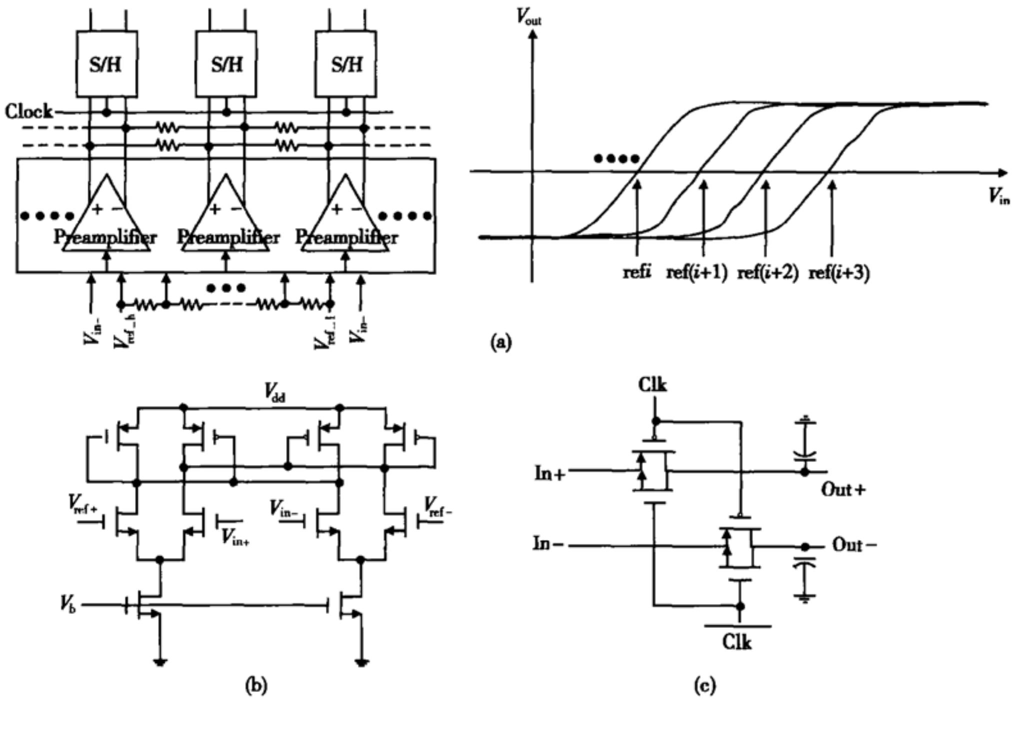

Fig. 2 (a) Distributed track-and-hold amplifier array with resistor averaging; (b) Circuit diagram of the preamplifier; (c) Circuit diagram of the S/H

The preamplifier array is shown in Fig. 2. With the current sources replacing the resistor loads[4], the amplifier essentially turns into a transconductor that has a high gain. The S/H circuit consists of CMOS switch and capacitor. The capacitor can be implemented with MOS transistor because the linearity is not a very stringent requirement. The technique of averaging is used by inserting lateral resistors between the outputs of neighboring individual amplifiers. A low value is chosen for the lateral resistors, still yielding a reasonable gain (four to five times)[4].

The folder block is composed of several source coupled pairs, their tail-current sources, and two differential resistor loads, as shown in Fig. 3. The input signals of the folding block are amplified first and the output is folded current. In order to drive a voltage interpolating block, the resistor load plays

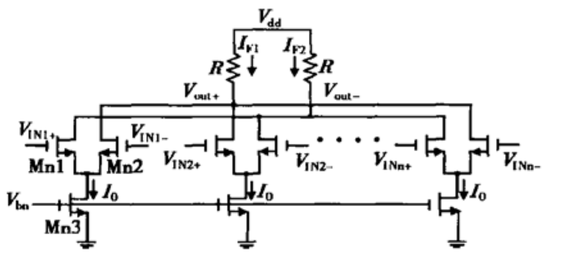

Fig. 3　Basic CMOS folding amplifier

the role to obtain the voltage output[6~8], $V_{out+} = V_{dd} - I_{F1}R$, $V_{out-} = V_{dd} - I_{F2}R$. Then the common voltage of the output and the gain can be expressed as

$$\frac{V_{out+} + V_{out-}}{2} = V_{dd} - \frac{R}{2}(I_{F1} + I_{F2}) = V_{dd} - \frac{nR}{2}I_0 \quad (1)$$

$$A_V = g_{Mn1}R \quad (2)$$

where g_{Mn1} is the transconductance of transistor Mn1. From Eqs. (1) and (2), the power and the resistor have direct effects on the output voltage and the gain. In a standard CMOS process, the resistor has even about 20% mismatches that can make a big deviation of the output voltage and the gain. This will be a stringent requirement for the following circuits to adapt to a large input range.

Figure 4 shows the resistor interpolation. Intermediate folded signals are produced after interpolation block. Usually, the interpolating voltages are buffered to prevent them from being perturbed by the nonlinearity of other ones through the interpolating network.

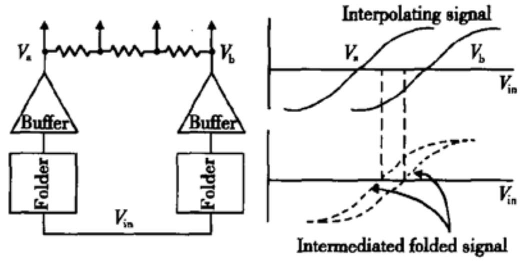

Fig. 4　Resistor interpolating

3　Improvement of the circuit design

3.1　Proposed folder

The output voltage and the gain have a large deviation in the conventional folder. To solve this problem, a modified folding circuit with MOS transistors completely replacing the resistor is proposed, as shown in Fig. 5. Most of the DC current flows from current source I_{bp} to reduce the power dissipation, $I_c = I_{F1} - I_{bp}$, $I_d = I_{F2} - I_{bp}$. The folded AC currents at Mp3 and Mp4 are mirrored at Mp5 and Mp6 with a gain M, $I_{out+} = MI_c$, $I_{out-} = MI_d$. Mn5 and Mn6 are current-to-voltage converters. The output voltage can be obtained as the following:

$$V_{out+} = \sqrt{2M(I_{F1} - I_{bp}) \Big/ \left[\mu_n C_{ox}\left(\frac{W}{L}\right)_{n5}\right]} + V_{TN} \quad (3)$$

$$V_{out-} = \sqrt{2M(I_{F2} - I_{bp}) \Big/ \left[\mu_n C_{ox}\left(\frac{W}{L}\right)_{n6}\right]} + V_{TN} \quad (4)$$

where μ_n is the mobility of electrons, and C_{ox} is the gate capacitance per unit area. V_{TN} is the NMOS transistor threshold voltage. In the circuit design, Mn5 and Mn6 are set with the same sizes $(W/L)_{n5} = (W/L)_{n6}$. From Eqs. (3) and (4), the new functions of the common voltage can be given as

$$\frac{V_{out+} + V_{out-}}{2} = \sqrt{M \Big/ \left[2\mu_n C_{ox}\left(\frac{W}{L}\right)_{n5}\right]} \times \left(\sqrt{I_{F1} - I_{bp}} + \sqrt{I_{F2} - I_{bp}}\right) + V_{TN} \quad (5)$$

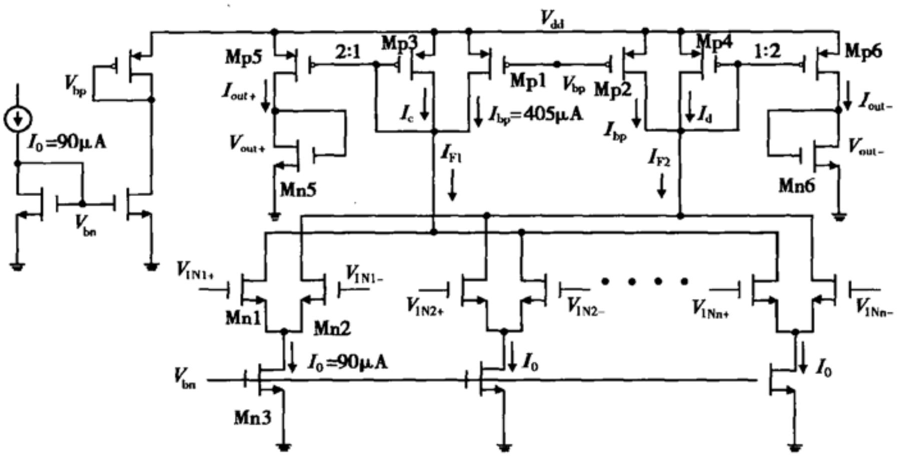

Fig. 5 Proposed folder circuit

Now, the gain can be expressed as $A_V = Mg_{Mn1}/g_{Mn5}$, where g_{Mn5} is the transconductance of transistor Mn5, $g_{Mn1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{n1} \times \left(\frac{I_0}{2}\right)}$, $g_{Mn5} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{n5} \times M \times \left(\frac{nI_0}{2} - I_{bp}\right)}$. By replacing g_{Mn1} and g_{Mn5}, the following function can be deduced

$$A_V = \sqrt{\frac{MI_0}{nI_0 - 2I_{bp}} \times \frac{(W/L)_{n1}}{(W/L)_{n5}}} \quad (6)$$

The proposed folder and a conventional folder with resistor loads were designed and simulated in the same model (0.18μm 3.3V CMOS). Figure 6 shows the comparison results. When the power supply changes from 2.7V to 4.0V, the output common voltage has only 1% deviation for the proposed folder while it is 98.4% for the conventional one. The gain of the proposed folder has 9% deviation which is more than that of the conventional one, 2%. But if the resistor value mismatch (±10%) is considered, the gain deviation will be 22%. So the proposed folder has a better power-supply rejection capability. Furthermore, to get the same gain under 3.3V power supply, the power dissipation of the conventional folder is 5.5mW and it is 5.0mW for the proposed one. Because the load is composed of transistors, not resistor, the area and parasitic effect of the proposed folder will be also reduced. In the circuit design, I_0 is set to 90μA, I_{bp} is 405μA, and M is 2.

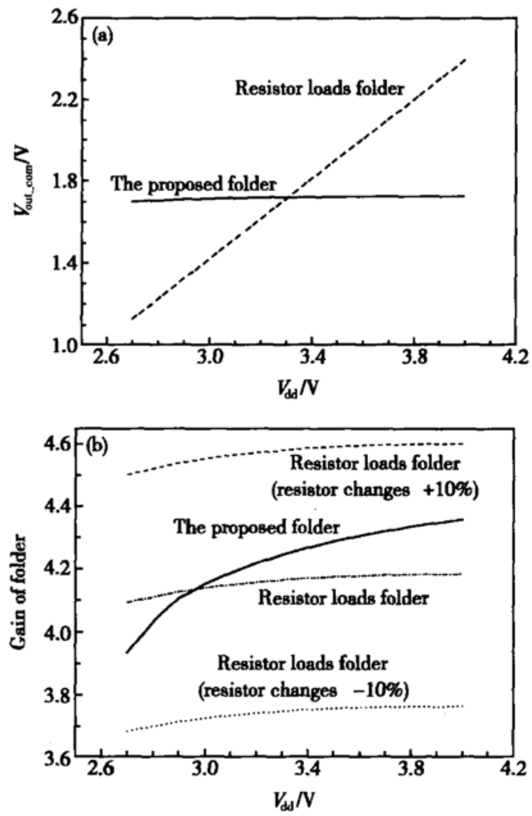

Fig. 6 Folders comparison (a) Output common voltage; (b) Gain versus the power supply

3.2 Proposed comparator

The comparator transfers the output of interpolating block to digital signal, which is sent to drive the digital encoder block. The output of the comparator becomes "high" or "low" according to the differential input voltage level. Response time from the beginning of comparing to outputting "high" or "low" is decided by both the comparator itself and the differential value of input voltage. The proposed comparator is shown in Fig. 7. It has an operation with high speed without a kickback effect[2]. The gate capacitors of Mn8 and Mn9 have no change at the time the comparator moves from "Reset" to "Compare" because the voltage between gate and source keeps stable. Then the differential value between two voltages on the gates of Mn8 and Mn9 does not change to obtain a small response time, comparing with the comparator[2].

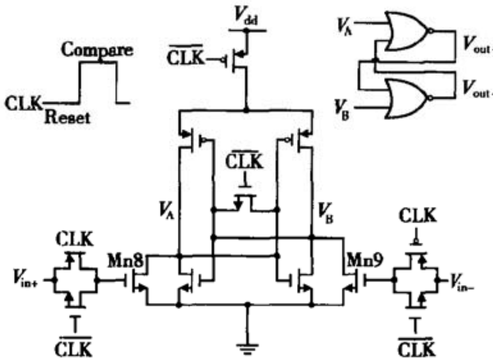

Fig. 7 Circuit diagram of the proposed comparator

4 Simulation results

The circuit is simulated with a 3.3V spice model in 0.18μm digital CMOS technology. The core layout of ADC is presented in Fig. 8, occupying an active area 475μm×526μm= 0.25mm^2. Figure 9 shows the simulation results of SNDR and SFDR versus analog input frequency at the sampling rate of 200MHz. The ADC has an nearly ideal ENOB until the analog input frequency increases to 10MHz. The total power dissipation is 177mW at 200Ms/s and 32mW is for the digital part. The simulation performances are summarized in Table 1. Table 2 shows a performance comparison between those conventional flash ADCs recently published and this work that is competitive.

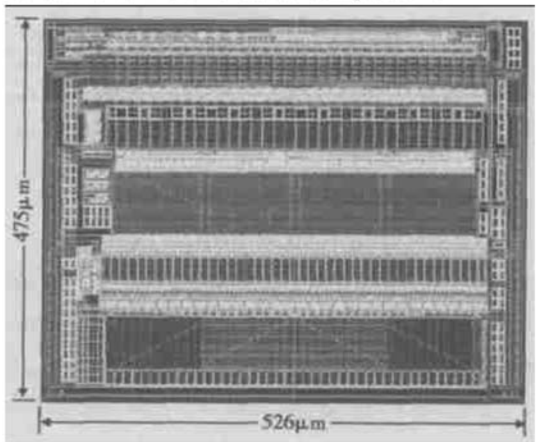

Fig. 8 Core layout of ADC

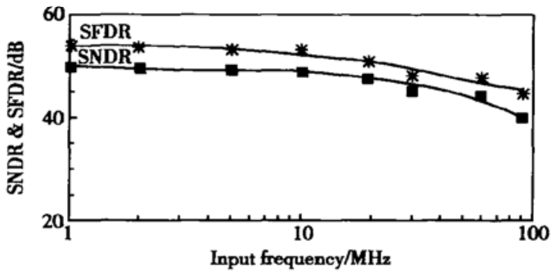

Fig. 9 Simulated SNDR and SFDR versus analog input frequency at 200MHz conversion rate

Table 1 Summary of ADC performance

Process	0.18μm standard CMOS
Resolution	8bit
Conversion rate	200MHz
Supply voltage	3.3V
Input range	1.92V_p(differential)
SNDR/SFDR	49.2dB/53.2dB(f_{in}= 10MHz)
(f_{clk}= 200MHz)	44.2dB/47.8dB(f_{in}= 60MHz)
Power dissipation	177mW
Active area	0.25mm^2

Table 2 ADC comparison

Author	Process	Area/mm^2	Bits	Power/mW	Conversion rate /MHz	Power/Speed /(mW·MHz^{-1})
This work	0.18μm CMOS	0.25	8	177	200	0.885
Irie[9]	Bipolar	5.5	8	950	500	1.9
Uyttenhove[10]	0.35μm CMOS	3.36	8	655	200	3.275
Kim[2]	0.35μm CMOS	0.96	8	210	200	1.05
Feygin[11]	0.18μm CMOS	0.9	8	140	165	0.85

续表 2

Author	Process	Area/mm^2	Bits	Power/mW	Conversion rate /MHz	Power/Speed /(mW·MHz^{-1})
Wang[12]	0.6μm CMOS	1.8	8	395	150	2.63
Yoon[1]	0.35μm CMOS	0.8	8	110	125	0.88
Choe[7]	0.5μm CMOS	1.68	8	165	100	1.65
Ming[13]	0.5μm CMOS	10.3	8	268	80	3.35
Hughes[14]	0.35μm CMOS	0.62	8	60	40	1.5

5 Conclusion

A 3.3V 8bit 200Ms/s folding and interpolating CMOS ADC is designed in this paper. It is composed of both a coarse ADC and a fine ADC. In the fine ADC, a folding block with MOS transistor completely replacing the resistor is used to reduce the output voltage deviation and the area. The ADC is realized in standard digital 0.18μm 3.3V CMOS technology. A low power consumption 177mW and a small area 0.25mm^2 make this ADC very suitable for embedded application.

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200Ms/s 177mW 8 位折叠内插结构的 CMOS 模数转换器*

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摘要：介绍了一个采用折叠内插结构的 CMOS 模数转换器，适合于嵌入式应用．该电路与标准的数字工艺完全兼容，经过改进的无需电阻就能实现的折叠模块有助于减小芯片面积．在输入级，失调平均技术降低了输入电容，而分布式采样保持电路的运用则提高了信号与噪声的失真比．该 200MHz 采样频率 8 位折叠内插结构的 CMOS 模数转换器在 3.3V 电源电压下，总功耗为 177mW，用 0.18μm 3.3V 标准数字工艺实现．

关键词：模数转换器；CMOS 模拟集成电路；折叠内插

EEACC：1265H；1280；2570D

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