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A Novel LDMOS Structure in Thin Film Patterned-SOI Technology with a Silicon Window Beneath p Well*

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Abstract: A novel patterned-SOI LDMOS structure with a silicon window beneath the p well is proposed. The performance is simulated numerically. In comparison to SOI counterpart, the off-state and the on-state breakdown voltage can increase by 57% and 70% respectively; transconductance is flatter; *I*-*V* curves take no sign of kink in the saturation region; the device temperature is much lower even at high input power; the floating body effect and the self-heating effect are distinctly suppressed. Furthermore, the advantage of low leakage current and low output capacitance in SOI structures does not degrade. The proposed structure will be a promising choice to improve the performance and reliability of SOI power device.

Key words: patterned-SOI; LDMOS; floating body effect; self-heating effect
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1 Introduciton

Lateral double diffused MOS (LDMOSFET) has been a popular candidate in power amplifier applications. But high parasitic output capacitance and leakage current on bulk substrate will result in lower power gain and power aided efficiency. Silicon-on-insulator (SOI) LDMOSFET has much lower parasitic output capacitance and leakage current, making it a better candidate for high frequency application[1~4]. However, buried oxide layer results in generated holes due to impact ionization accumulating in neutral p body region, and the threshold voltage decreases, with leading to serious floating body effect in the partially-depleted SOI device, such as the kink in the *I*-*V* characteristics which gives rise to distortion during power operation and produces poor power efficiency[5]. In addition, buried oxide layer has a relatively small heat conductivity coefficient, so the generated heat cannot easily flow to the substrate, and the device temperature rises, resulting in a serious self-heating effect, such as the degradation of carriers mobility[6].

Body contact technology[7], shallow source implantation technology[8], and patterned-SOI technology[9,10] are suggested to eliminate floating body effect. However, body contact can reduce gate width effectivly, and shallow source implantation need careful process control especially for thin-film SOI structure. Ren *et al.*[9] fabricated a patterned-SOI LDMOSFET without buried oxide beneath the source and p well regions, resulting in poor isolation between adjacent circuits. In addition, the pro-

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cess to form patterned-SOI materials is too complex to be accepted widely. Park *et al.*[10] simulated a patterned-SOI structure without buried oxide underneath the drain region, which increases leakage current and parasitic output capacitance.

In this paper, a novel patterned-SOI (PSOI) LDMOSFET structure is proposed. Buried oxide is interrupted beneath p well region, existing under source region and drain region. The region where buried oxide is interrupted is called silicon window. PSOI materials can be realized easily by masked separation by implantation of oxygen (SIMOX) technology[11]. This structure can overcome described drawbacks of conventional PSOI structures.

2 Process simulation and model description

The cross-section of the proposed PSOI LDMOSFET is shown in Fig. 1. The main process to form PSOI materials are illustrated in Fig. 2. Thick thermal SiO_2 is grown on p-type wafer and etched selectively where buried oxide layer will be formed, then oxygen ion is implanted and annealed. The top silicon thickness is 0.2μm, the buried oxide layer thickness is 0.4μm, and the length of silicon window is 0.8μm. 30nm gate oxide is thermally grown on the patterned-SOI wafer. Poly-silicon is deposited, doped and patterned. Boron ion ($1.5\times10^{13}cm^{-2}$, 35keV) is implanted into the source region, then annealed for 2h at 1150℃ to form p well doping. The drift region doping is achieved by a blanket implantation of phosphorus ($2\times10^{12}cm^{-2}$, 50keV according to the RESURF rules[12]) and anneal. Oxide is deposited by TEOS and etched selectively to define drift region and to form spacer wall. After the source and drain regions are made by phosphorus ion implantation, a titanium salicide is performed. The process is simulated by TSUPREM4[13]. The finally effective channel length is 0.7μm, and the drift region length is 0.5μm.

Electrothermal characteristics are simulated

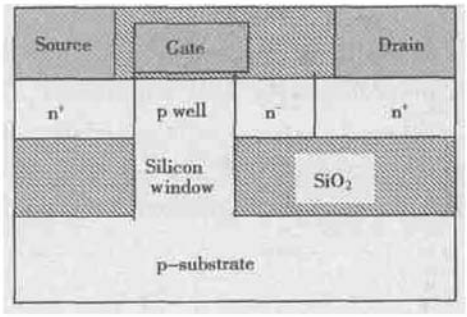

Fig. 1　Cross-section of patterned-SOI LDMOSFET

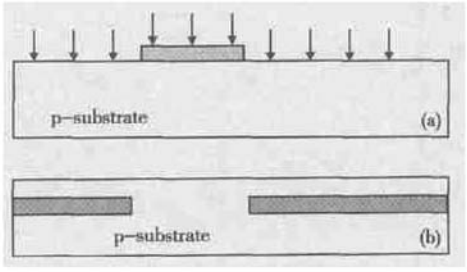

Fig. 2　Proposed process sequences for PSOI formation (a) Selective O^+ implantation, thermal oxide as mask; (b) High temperature annealing and buried oxide formation

by MEDICI[14] on PSOI structure and SOI counterpart. The following models are used in the simulation: Shockley-Read-Hall recombination model with concentration dependent lifetimes (CONSRH); Auger recombination model (AUGER), carrier generation due to impact ionization is included in the solution self-consistently (IMPACT.I); concentration and temperature dependent mobility model (ANALYTIC), an enhanced surface mobility model accounting for phonon scattering, surface roughness scattering, and charged impurity scattering (SRFMOB2); the mobility model using the parallel electric field component (FLDMOB). The simulation results are compared to reported experimental data[4] in order to verify the effectiveness of chosen models.

3 Results and discussion

3.1 Drain leakage current and off-state breakdown voltage

Figure 3(a) shows off-state I-V characteris-

tics. Drain leakage current of PSOI device before breakdown is almost the same as that of SOI counterpart. In addition, PSOI device enables 57% increase in the off-state breakdown voltage from 14 to 22V compared to SOI device. The simulation value of the off-state breakdown voltage for SOI

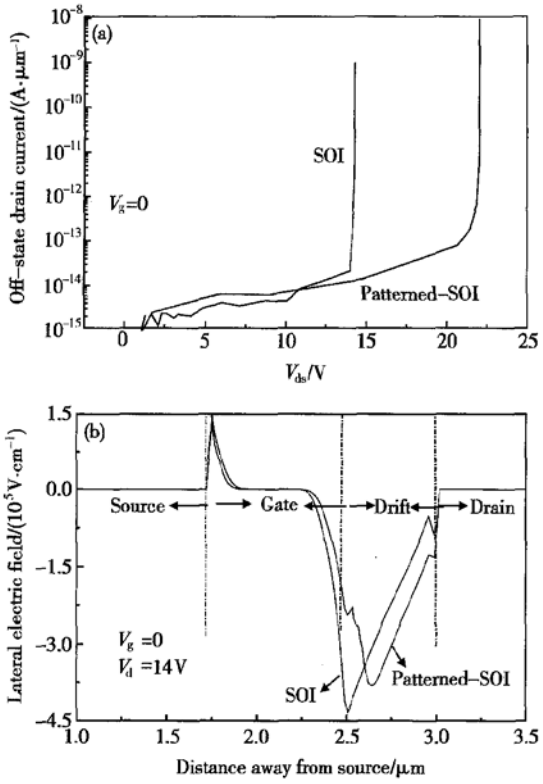

Fig. 3 (a) Off-state I-V characteristics; (b) Lateral electric field distribution along the device surface

counterpart is similar to the measured value in the literature[4]. The lateral electric field distributions are shown in Fig. 3(b). The field peak of PSOI is lower than that of SOI at the p well/n drift junction and moves to the internal of the drift region, which is beneficial to reduce the probability of the junction breakdown. In addition, the electric field in the drift region is more uniformly distributed to PSOI device, and the RESURF condition is satisfied to some extent. Consequently, the drift region can handle higher drain breakdown voltage. The other reason for higher blocking capability is that the parasitic bipolar transistor is not triggered until higher drain bias due to lower p body potential in PSOI structure.

3.2 Transfer characteristics

It can be seen from Fig. 4 that the current driving capability of PSOI structure is not good as that of SOI counterpart. This is due to lower threshold voltage in SOI ($V_{th,SOI}$) counterpart. $V_{th,SOI}$ is a little lower than that of PSOI structure even though p well doping is the same, and it also can decrease due to higher floating body potential. But it is also found that transconductance in SOI structure quickly decrease and will become lower than that of PSOI structure when the gate bias is beyond 4.2V. In SOI structure, generated Joule heat results in the rise of device temperature and the degradation of carrier mobility at higher gate bias, then drain current can not increase linearly with the change of gate bias, thus, transconductance quickly decreases. In PSOI structure, the silicon window allows heat to flow to substrate, and carrier mobility does not degrade. Consequently, drain current can rise linearly with the gate voltage to keep g_m flatter. Flat transconductance is beneficial to improve the device stability and the power gain.

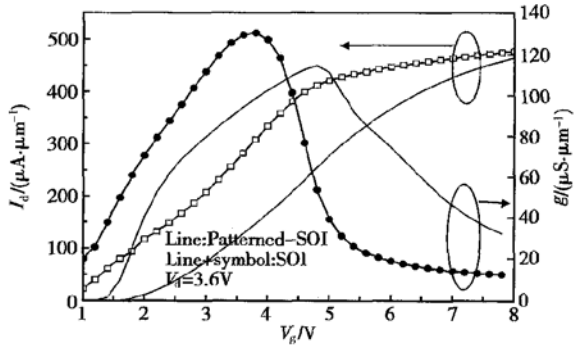

Fig. 4 Transfer characteristics

3.3 On-state output characteristics

The I-V output characteristics are shown in Fig. 5. The I-V curves keep flat until breakdown takes place and no sign of kink effect is shown in PSOI device. However, SOI counterpart exhibits a pronounced kink even at small drain voltage of 3V, which is identical to the experimental data[4]. In ad-

dition, the on-state breakdown voltage of PSOI device is higher than that of SOI counterpart, which is 12V at the gate bias of 3V, but only 7V in SOI counterpart, increased by 70%. In PSOI structure, a silicon window allows generated holes due to impact ionization flowing to the substrate, the neutral p body potential does not increase, and the threshold voltage does not change, therefore, no kink effect occurs in I-V curves. Lower p body potential also leads to the trigger of parasitic bipolar transistor at higher drain bias, therefore, PSOI can handle higher on-state breakdown voltage.

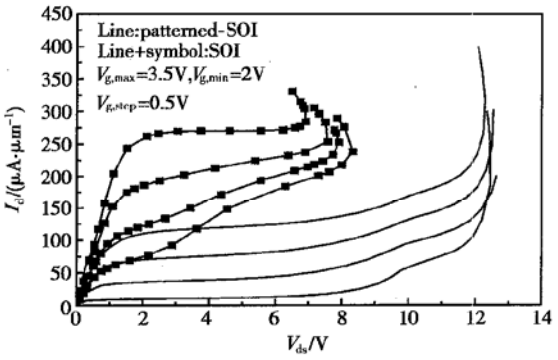

Fig. 5　On-state I-V characteristics with the gate voltage changing from 2V to 3.5V

In I-V curves of SOI structure, the kink is not distinct when the gate bias becomes high, even a little negative conductance appears at the gate bias of 3.5V. This is because that the degradation of carrier mobility counteracts the floating body effect. It is obvious that PSOI structure can suppress the self-heating effect.

3.4 Device temperature

Figure 6 is the device temperature distribution when the gate bias is 8V and the drain bias is 3.6V. The maximal temperature in PSOI device is 340K, about 100K lower than that of SOI counterpart. Hence, the carrier mobility does not degrade and self-heating effect is suppressed.

3.5 Output capacitance analysis

Output capacitance (C_{oss}) illustrated in Fig. 7

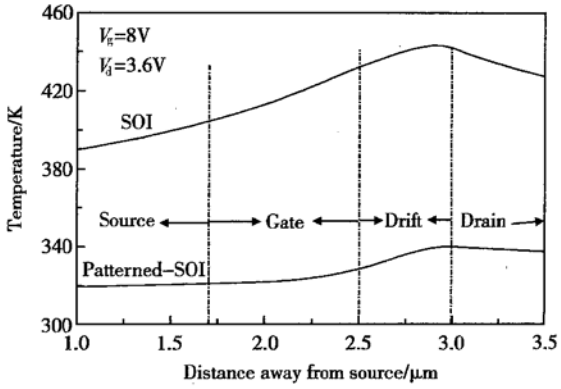

Fig. 6　Device temperature distribution along the device surface

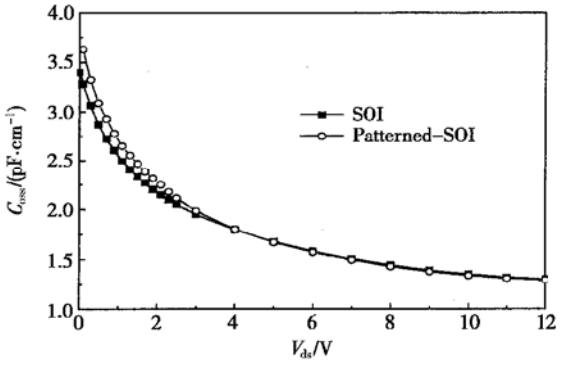

Fig. 7　Simulated C_{oss} versus V_d at V_g= 0V and 1MHz

is almost the same for both PSOI and SOI structures. C_{oss} is the capacitance between the drain and the source terminals with gate short-circuited to the source terminal. It can be treated as the combination of the gate-to-drain capacitance C_{gd}, the drain-to-source capacitance C_{ds}, and the drain-to-substrate capacitance C_{dsub}:

$$C_{oss} = C_{gd} + C_{ds} + C_{dsub} \tag{1}$$

$$C_{ds} = C_{js} \tag{2}$$

$$C_{dsub} = \frac{C_{ox}C_{jb}}{C_{ox} + C_{jb}} \tag{3}$$

C_{js} is n- drift/p well junction capacitance, C_{ox} is buried oxide layer capacitance, and C_{jb} is the depletion capacitance in the substrate. When drain voltage increases, an inversion layer appears beneath the buried oxide layer, preventing further depletion of the substrate, thus C_{jb} is fixed, and C_{oss} does not change with drain bias any more. Seen from Fig. 1, C_{js}, C_{gd}, C_{ox}, and C_{jb} are almost the same for SOI

and PSOI structures. Therefore, a silicon window only beneath the p well does not affect the advantage of low and flat output capacitance in SOI structures.

4 Conclusion

The proposed PSOI LDMOSFET structure with a silicon window beneath the p well is numerically analyzed. This structure has perfect performance compared to SOI counterpart, the off-state and the on-state breakdown voltages are improved by 57% and 70% respectively. Transconductance keeps flat within the wide range of gate voltage, no kink takes place in the I-V curves, and the device temperature is about 100K lower. Simulation results on SOI counterpart are similar to reported experimental data, therefore, the chosen models in numerical simulation are valid. The proposed PSOI structure is a promising technology platform to solve self-heating effect and floating body effect existing in SOI structures.

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新型图形化 SOI LDMOS 结构的性能分析*

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摘要：提出一种图形化 SOI LDMOSFET 结构，埋氧层在器件沟道下方是断开的，只存在于源区和漏区. 数值模拟结果表明，相对于无体连接的 SOI 器件，此结构的关态和开态击穿电压可分别提高 57% 和 70%，跨导平滑，开态 I–V 曲线没有翘曲现象，器件温度低 100K 左右，同时此结构还具有低的泄漏电流和输出电容. 沟道下方开硅窗口可明显抑制 SOI 器件的浮体效应和自加热效应. 此结构具有提高 SOI 功率器件性能和稳定性的开发潜力.

关键词：图形化 SOI；LDMOS；浮体效应；自加热效应

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