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10Gbps Transimpedance Amplifier for Optoelectronic Receivers Based on InGaP/GaAs HBTs*

Yuan Zhipeng, Sun Haifeng, Liu Xinyu and Wu Dexin

(*Institute of Microelectronics, The Chinese Academy of Sciences, Beijing 100029, China*)

Abstract: A transimpedance amplifier based on InGaP/GaAs HBTs, which is applicable for 10Gbps bit rate, is developed and realized. Compact chip layout guarantees good flat gain, linear phase, and small group delay time variation. Measured transimpedance gain is 40 dB · Ω and 3dB bandwidth is 10GHz.

Key words: TIA; HBT; 10Gbps; InGaP

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1 Introduction

Two possible ways exist for very high bit rate fiber optic links. Firstly, electrical time domain multiplexing (ETDM) used for ultra high bit rate (≥40Gbps) optoelectronic receivers (and transmitters) has been demonstrated in Ref. [1] recently. Alternatively, optical wavelength division multiplexing (WDM) can be applied for $n \times 10$Gbps, where n is the number of simultaneously used optical wavelengths on a fiber.

In this paper we report on the development and the technological realization of an amplifier suitable for WDM applications with bit rate up to 10Gbps. This amplifier chip is part of a module comprising a pin-diode for 1.55μm wavelength detector and the amplifier, both mounted on a subcarrier.

2 HBT devices characteristics and MMIC process

The MMIC is based on the 100mm InGaP/GaAs HBT device technology with an emitter finger width of 3.6μm. The epitaxial layer structure is shown in Table 1. Two metal layers are provided for interconnection. 25Ω/□ NiCr is used for thin-film resistors. Metal-insulator-metal (MIM) capacitors are realized with PECVD Si_3N_4 with a unit capacitance of 180pF/mm^2.

Table 1　Epitaxial layer structure

Layer number	Epitaxy composition	Thickness /nm	Carrier type	Carrier conc. /cm^{-3}
0	GaAs	(625±25)μm	N/A	N/A
1	GaAs	500	n^+	5×10^{18}(Si)
2	GaAs	500	n^-	3×10^{16}(Si)
3	GaAs	60	p^{++}	4×10^{19}(C)
4	InGaP(x= 0.5)	50	n	3×10^{17}(Si)
5	GaAs	120	n^+	5×10^{18}(Si)
6	$In_xGa_{1-x}As$	50	n^{++}	$> 10^{19}$(Si)
7	$In_{0.6}Ga_{0.6}As$	50	n^{++}	$> 10^{19}$(Si)

The measured HBT dc current gain is approximately 80 at a current density of J_c= 40kA/cm^2. The common-emitter breakdown voltage BV_{CEO} is 10V. The 3.6μm×6μm single-emitter HBTs used in design achieves an f_T of 60GHz at collector-emitter voltage (V_{CE}) of 2V. The HBTs have been

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Yuan Zhipeng　male, was born in 1973. His interests are compound semiconductor devices and MMICs.

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modeled with VBIC model. Deviations between simulation and measurement of dc and S-parameter data are very small (cf. Figs. 1 and 2) even for a wide range of bias points.

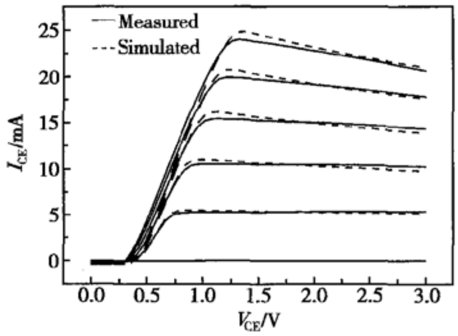

Fig. 1 Measured and Simulated dc output characteristics of the HBT with VBIC model

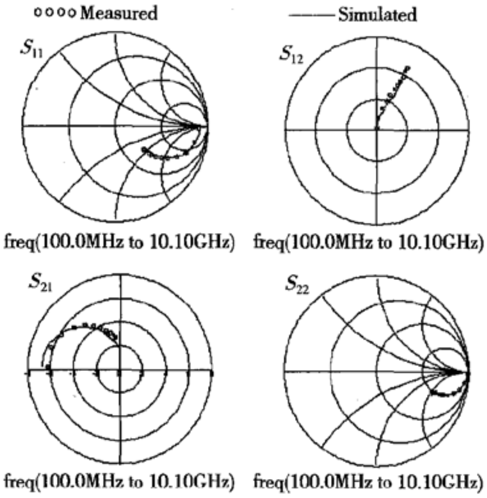

Fig. 2 Measured and simulated S-parameter of the HBT with VBIC model

3 Circuit design and realization

The circuit diagram of the amplifier is depicted in Fig. 3. The first stage is the cascade structure. It is the most popular structure[2,3] because of its high gain and wide bandwidth. The first stage is followed by limiting amplifier which used cherry hooper differential amplifier[4] and a 50Ω differential output buffer stage. The Cherry-Hooper structure reduces the Miller component of the input capacitance and is advantageous to the bandwidth of the LA stage. All the HBT transistors are biased at or below a conservative current density of $0.8{\rm mA}/\mu{\rm m}^2$ in order to insure reliable operation. The TIA is operated at 5V and draws 140mA for a total power consumption of about 700mW. The chip size is 1.2mm × 1.2mm.

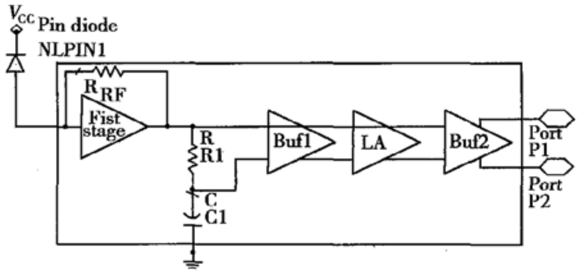

Fig. 3 Circuit diagram of transimpedance amplifier

4 Results

On-wafer small-signal S-parameter measurements are performed to assess the amplifier performance using coplanar probes. Figure 6 shows the small-signal measurement set-up[5]. It is composed by a transimpedance amplifier, a test board with lumped components, and a HP 8510 MWA with 50Ω of input impedance. The photodiode is modeled by 1kΩ resistor (to transform the voltage generator into current generator) and a shunt 0.3pF capacitor. An external bias-T is added between the HB 8510 NWA and the transimpedance amplifier. Throught the bias-T, we applied a dc forward current ($I_{\rm d\text{-}dc}$), which is equal to ($V_{\rm in}-V_{\rm ref}$)/$R_{\rm p}$, where $V_{\rm ref}$ is a dc voltage at the input of the TIA. The output reflection coefficient is better than − 7dB over the bandwidth of operation (see in Fig. 4). The effective transimpedance gain ($|Z_{\rm eff}|$) is calculated from the measured small-signal S-parameters using Eq. (1) for $Z_0 = 50\Omega$[6], and shows a flat gain of 40dB • Ω over a bandwidth of 10GHz (see in Fig. 5). The noise figure is about 7dB calculated from the measured small-signal S-parameters[7,8]. Figure 7 shows the photograph of a completed TIA chip.

$$|Z_{\rm eff}| = Z_0 \times \frac{|S_{21}|}{|1 - S_{11}|} \qquad (1)$$

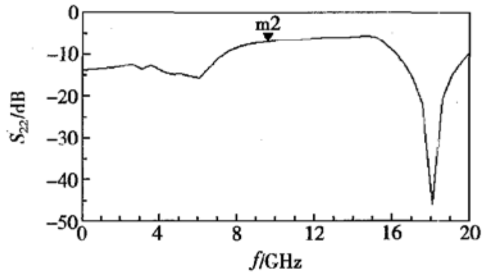

Fig. 4 Output reflection $S_{22}< -7$dB for $f<10$GHz

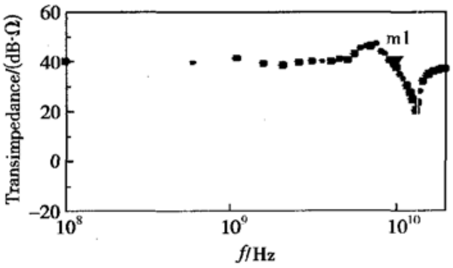

Fig. 5 Transimpedance gain based on TIA *S*-parameters

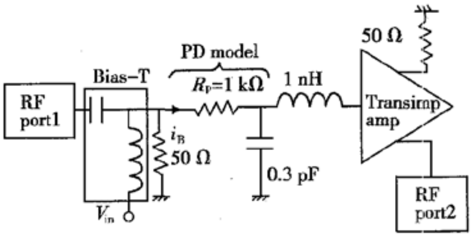

Fig. 6 Small-signal measurement set-up

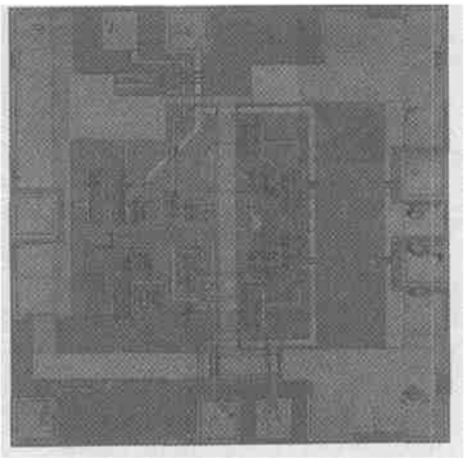

Fig. 7 TIA chip

5 Conclusion

Overall, a high-bandwidth transimpedance amplifier is designed, fabricated, and tested. This amplifier can be employed in high-speed, medium to long-haul optoelectronic receivers. Simplicity in fabrication, high yield, high reliability, and high performance are some advantages of the technology employed for its fabrication.

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基于 InGaP/GaAs HBT 的 10Gbps 跨阻放大器*

袁志鹏　孙海锋　刘新宇　吴德馨

(中国科学院微电子研究所，北京　100029)

摘要：采用 InGaP/GaAs HBTs 设计并实现了传输速率为 10Gbps 的跨阻放大器.在电路设计上采用两级放大器级联的形式以提高跨阻增益,在第一级采用了 cascade 结构,第二级采用了 cherry hooper 结构以提高电路的带宽和稳定性.测试结果表明,跨阻增益为 40dB·Ω,3dB 带宽为 10GHz.

关键词：跨阻放大器；HBT；10Gbps；InGaP

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袁志鹏　男,1973 年出生,博士研究生,主要从事化合物半导体器件和微波单片集成电路等方面的研究.

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