第 25 卷第 12 期 半 导 体 学 报 Vol. 25, No. 12
2004 年 12 月 CHINESE JOURNAL OF SEMICONDUCTORS Dec., 2004

Optimization and Synthesis of RF CMOS Polyphase Filters with Layout Considerations

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Abstract: A novel software tool for optimization and synthesis of RF CMOS polyhase filters(PPFs), PPFOPTIMA, is developed. In the optimization engine, genetic algorithm is adopted to avoid local optima. Experiments on PPFOPTIMA demonstrate that it is an efficient design aid for design and optimization of RF CMOS PPFs.

Key words: RF CMOS; polyphase filters; quadrature signal generation; genetic algorithms; analog CAD
EEACC: 2520M; 2560J; 1350J
CLC number: TN405 **Document code**: A **Article ID**: 0253-4177(2004) 12-1612-06

1 Introduction

Quadrature signal generation is an important function block in modern wireless transceivers in which quadrature modulation and demodulation are widely applied. However, some quadrature signal generation techniques are not well suited for CMOS implementation because complicated tuning circuits are needed to overcome CMOS process tolerances. Polyphase filters (PPFs), originally developed for single-side band modulation in audio frequency[1], have been rediscovered as an efficient solution for high accuracy quadrature generation in radio frequency CMOS designs[2] because of its simple stagger-tuning mechanism and robustness to CMOS process tolerance.

Previous works were concentrated on analysis[3] and design of RF CMOS PPFs. Some design guidelines were presented by Behbahani[4]. However, they give too much freedom for the design, and it needs intensive trials and several design cycles to reach a good design. With layout considerations, optimization of RF CMOS PPFs can not be solved by using analytical mathematics, because of multiple design objectives and constraints. PPFOPTIMA, a novel software tool for optimization and synthesis of RF CMOS PPFs, has been developed. In the optimization engine, genetic algorithm(GA) is adopted to avoid local optima. Experiments on PPFOPTIMA demonstrate that it is an efficient design aid for design and optimization of RF CMOS PPFs.

2 Considerations in schematic design

As is well known, CMOS process has severe process tolerances. In the design of RF CMOS PPFs, process tolerances can be overcome by using the concept of "folerance design". Specifically, by enlarging the bandwidth of the polyphase filters, the worst-case bandwidth of the polyphase filters can be guaranteed to be located in the operating band, which is the principle of stagger-tuning technique. In Fig. 1, gain mismatches (gain difference between I path and Q path) influenced by process tolerances in an RF CMOS PPF designed for a

Received 20 February 2004, revised manuscript received 24 July 2004

bluetooth receiver are shown, from which we can see that, no matter how R_s and C_s vary (within process tolerance), the operating frequency band of bluetooth signal (2.4~ 2.48GHz) is always covered.

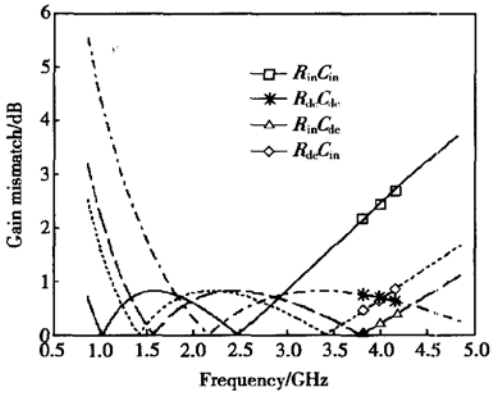

Fig. 1　Gain mismatch influenced by process tolerances in an RF CMOS PPF

3　Considerations in physical layout

In physical layout, component mismatch and parasitic effects have significant influences on the performance of RF CMOS PPFs. Even though there are some layout techniques such as inter-digitized structure, common centroid structure to minimize component mismatch, it can not be totally eliminated. The most important specification for an RF CMOS PPF is image reject ratio (IRR), which is related to the sensitivity of a receiver. From Monte Carlo simulations[4] it has been found that:

$$\mathrm{IRR_U} > -20\lg\sigma_{\mathrm{component}} \tag{1}$$

where $\mathrm{IRR_U}$ is the ultimately obtainable image reject ratio, and $\sigma_{\mathrm{component}}$ is the component mismatch. It is known from the experimental study[5] that the variance of adjacent on-chip resistors and capacitors is proportional to the inverse of their area, that is, neighboring components with larger area can be better matched. By using the latest resistor and capacitor mismatch models[5] as shown in Eqs. (2) and (3), the minimum area required by a given specification can be calculated.

$$\sigma^2_{\Delta R/R} = \sigma^2_{R_{\mathrm{sh}}} \times \left[\frac{L}{LR_{\mathrm{sh}} + R_{\mathrm{e}}}\right]^2 + \sigma R_{\mathrm{e}}^2 \times \left[\frac{L}{LR_{\mathrm{sh}} + R_{\mathrm{e}}}\right]^2 + \sigma^2_{\Delta W} \times \left[\frac{L}{W + \Delta W}\right]^2 \tag{2}$$

where $\sigma_{R_{\mathrm{sh}}} = \frac{A_{R_{\mathrm{sh}}}}{(WL)^{1/2}}$, $\sigma_{R_{\mathrm{e}}} = A_{R_{\mathrm{e}}}$, $\sigma_{\Delta W} = \frac{A_{\Delta W}}{W^{1/\sqrt{2}}}$, σ is the standard deviation, W and L are resistor width and length, R_{sh} is the sheet resistance of the polysilicon resistor, R_{e} is the end resistance coefficient, ΔW is the resistor width offset.

$$\sigma^2_{\Delta C/C} = \sigma^2_{\mathrm{p}} + \sigma^2_{\mathrm{a}} + \sigma^2_{\mathrm{d}} \tag{3}$$

where $\sigma_{\mathrm{p}} = \frac{f_{\mathrm{p}}}{C^{3/4}}$, $\sigma_{\mathrm{a}} = \frac{f_{\mathrm{a}}}{C^{1/2}}$, and $\sigma_{\mathrm{d}} = f_{\mathrm{d}}d$, f_{p}, f_{a}, f_{d} are constants describing the influences of periphery, area and distance fluctuations.

Optimized for digital circuits, CMOS process has severe parasitic effects which are quite challenges for analog design. In the design of RF CMOS polyphase filters, there are two effects from parasitics:

(1) Signal loss caused by the lossy substrate in addition to the theoretical - 3dB/stage in passive filters;

(2) Noise coupling caused by parasitic capacitance.

For a given CMOS process, there are two ways to minimize these effects. One is to minimize the chip area, the other is to use shieldings, namely N-wells and guard rings to protect noise sensitive analog circuits.

With considerations of parasitics, the maximum length of the resistor (MLR) allowed in a certain CMOS process can be derived as follows:

$$f_{\mathrm{R}} = \frac{1}{2\pi RC_{\mathrm{p}}} = \frac{1}{2\pi \times \frac{L}{W} \times LW\rho C_{\mathrm{p}}} = \frac{1}{2\pi L^2 \rho C_{\mathrm{p}}} \tag{4}$$

$$f_{\mathrm{op}} \leqslant f_{\mathrm{R}} = \frac{1}{2\pi L^2 \rho C_{\mathrm{p}}} \tag{5}$$

$$L \leqslant \frac{1}{\sqrt{2\pi f_{\mathrm{op}} \rho C_{\mathrm{p}}}} \tag{6}$$

where ρ is sheet resistance, L is the length of the resistor, and C_{p} is parasitic capacitance per unit area to the substrate. Before physical layout, the

MLR should be calculated.

4 Optimization problem formulation

In the design of RF CMOS PPFs, the design objectives are to:

(1) Satisfy the specifications required by corresponding wireless communication standard and transceiver architecture;

(2) Minimize chip area (thus parasitic capacitance between RF CMOS PPFs and the substrate can be minimized);

(3) Maximize immunity to noise coupling;

(4) Minimize additional signal loss.

Based on the design objectives, we can categorize previous design consideration as objective functions A and constraints B.

(A) Objective functions are IRR and chip area (Please note that an accurate IRR equation is used here).

$$\mathrm{IRR} = -20\lg\left(\frac{\Delta A^2}{16(A_I + A_Q)^2} + \frac{\Delta\phi^2}{4}\right) \quad (7)$$

where $\Delta A = |A_I - A_Q|$, $\Delta\phi = |\phi_I - \phi_Q|$, A_I, A_Q, ϕ_I, ϕ_Q are amplitudes and phases of I paths and Q paths respectively. They can be calculated by using transfer functions of PPFs[4].

Chip area (including dummies):

$$S = \sum_{i=1}^{n}(6S_{R_i} + 16S_{C_i}) \quad (8)$$

where $S_{R_i} = L_{R_i} \times W_{R_i}$, $S_{C_i} = \frac{C}{C_{\mathrm{unit}}}$, $i = 1, 2, \cdots, n$, L_{R_i}, W_{R_i} are the length and width of resistors in the ith stage respectively, C_{unit} is the unit capacitance of the capacitors.

(B) Design constraints: Even though chip area is to be minimized, for a given specification of IRR, there are minimum areas of resistors and capacitors to avoid intolerable component mismatch, they can be calculated by using Eqs. (9) and (10).

$$\sigma_{\Delta R/R} \geqslant 10^{-\mathrm{IRR}/20} \quad (9)$$

$$\sigma_{\Delta C/C} \geqslant 10^{-\mathrm{IRR}/20} \quad (10)$$

Another constraint in practice is that the length of resistors should be less than the maximum resistor length calculated by Eq. (6).

The optimization problem formulated above has multiple objectives, and furthermore the main objective function, IRR, was found to have multiple peaks. Traditional optimizations methodologies like calculus-based optimization, gradient descend are no longer suitable for this application, because they are subject to local optima. Under this situation, genetic algorithm has advantages over any other conventional optimization techniques for its capability in escaping from local optima, thus it is adopted in the optimization engine of PPFOPTIMA.

5 System implementation

Based on aforementioned design considerations in schematic and layout, a design flow for synthesis of RF CMOS PPFs has been proposed as shown in Fig. 2.

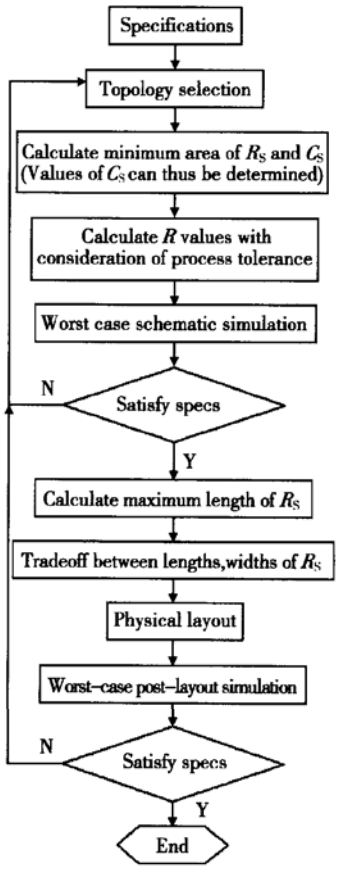

Fig. 2 A design flow for synthesis of RF CMOS PPFs

Different from other traditional optimization methods, the first step in using GA is to construct a fitness function, which is the criterion for selecting suitable population in the next generation. In PPFOPTIMA, the fitness function is a sum of IRR, chip area (S), and component mismatch property of resistors and capacitors with different weights as shown in Eq. (11).

$$F = w_1 S + w_2(\mathrm{CM}_R + \mathrm{CM}_C) + w_3\mathrm{IRR} \quad (11)$$

where w_1, w_2, and w_3 are the weights for chip area, component mismatch of resistors and capacitors, and IRR, respectively. In PPFOPTIMA, as S, CM_R, CM_C are in the order of 10^{-3}, w_1 and w_2 values are given in the order of 10^4 to differentiate good population from poor ones.

The framework of PPFOPTIMA is shown in Fig. 3, from which we can see that considerations in both schematic design and physical layout are incorporated into this software tool. Inputs needed from the user are the operating frequency and process related information, thus it is very convenient and efficient for novice designers under time-to-market pressures.

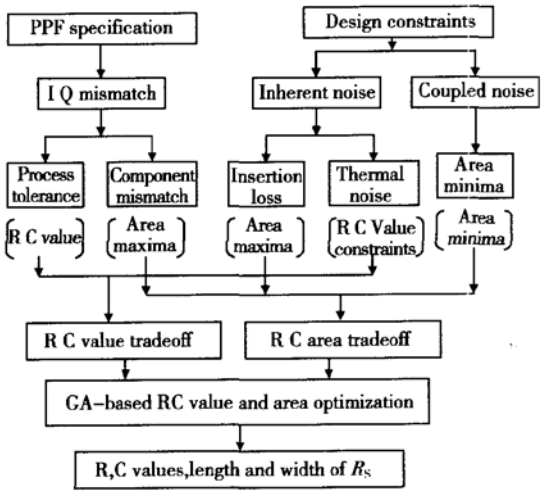

Fig. 3　Framework of PPFOPTIMA

6　Experiments on PPFOPTIMA

In order to design an RF CMOS PPF for a low-IF CMOS single-chip bluetooth receiver in Fraunhofer-IMS CMOS technology, a 2-stage and a 3-stage RF CMOS PPFs were synthesized by using PPFOPTIMA, and the synthesis results were compared and analyzed. The specifications derived from the bluetooth standard and the low-IF receiver architecture are following: gain mismatch (GM) ≤ 0.6dB, phase mismatch (PM) ≤5°. GM and phase difference (PD, please note that PM = PD − 90°) in RF CMOS PPFs synthesized are shown in Figs. 4 and 5 by using their transfer functions. From these figures, we can see that 3-stage RF CMOS PPFs has better quadrature accuracy (less GM and PM) than that 2-stage PPF has. Final design parameters and simulation results are shown in Tables 1 and 2 respectively (W stands for the widths of resistors

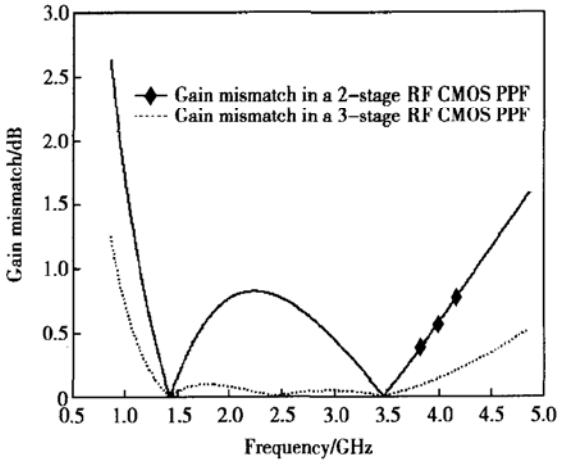

Fig. 4　Transfer function of multiple stages RF CMOS PPFs showing gain mismatch

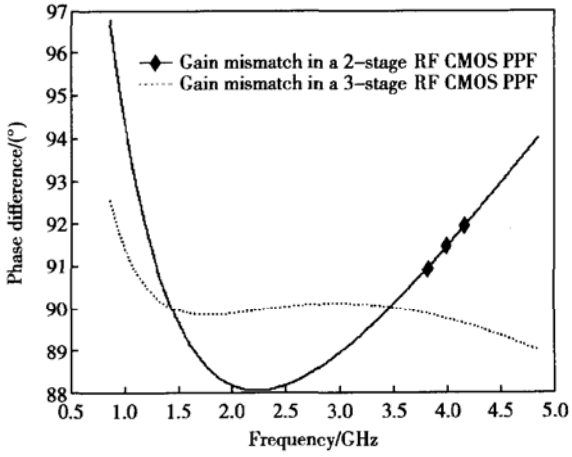

Fig. 5　Transfer function of multiple stages RF CMOS PPFs showing phase difference

in these tables). From Tables 1 and 2, we can see that, 3-stage PPF has better quadrature accuracy, but it has larger chip area and more insertion loss (IL) than that 2-stage PPF has. As both of them satisfy targeting specifications, 2-stage RF PPF was chosen by PPFOPTIMA. The schematic of the 2-stage RF CMOS PPF is shown in Fig. 6.

Table 1 Synthesis results of a 3-stage RF CMOS PPF by PPFOPTIMA

Component value				Simulation result				Chip area/μm^2
Resistor/Ω			$W/\mu m$	Capacitor/fF	GM/dB	PM/(°)	IL/dB	
R_1	R_2	R_3		229.4	0.07	0.26	-9.2	53912.8
271.6	283.6	347.6	3					

Table 2 Synthesis results of a 2-stage RF CMOS PPF by PPFOPTIMA

Component value					Simulation result			Chip area/μm^2
Resistor/Ω		$W/\mu m$	Capacitor/fF		GM/dB	PM/(°)	IL/dB	
R_1	R_2		C_1	C_2	0.18	0.45	-6.1	37525.6
223.5	256.6	3	238.9	312.9				

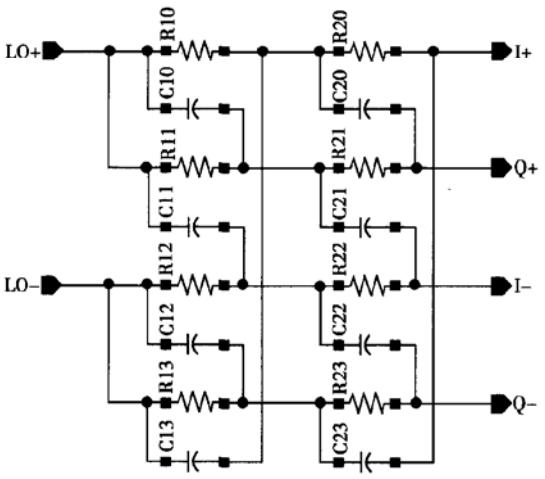

Fig. 6 Schematic of a 2-stage RF CMOS polyphase filter

7 Conclusion

In this paper, based on the design heuristics in schematic design and physical layout, PPFOPTIMA, an optimization and synthesis tool for RF CMOS polyphase filters, has been developed. Gentic algorithm was adopted in the optimization engine to avoid local optima. Experiments on PPFOPTIMA demonstrate that this software tool is efficient in design aid and optimization of RF CMOS PPFs.

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考虑布局因素的射频 CMOS 多相位滤波器的优化与合成

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摘要: 开发了一个新颖的考虑布局因素的用于射频 CMOS 多相位滤波器的优化和合成工具——PPFOPTIMA. 在优化引擎中使用了遗传算法用来避免局部的优化解. 实验结果证明 PPFOPTIMA 是射频 CMOS 多相位滤波器设计和优化中有效的计算机辅助设计工具.

关键词: 射频 CMOS; 多相位滤波器; 正交信号发生; 遗传算法; 模拟电路计算机辅助设计

EEACC: 2520M; 2560J; 1350J

中图分类号: TN405　　**文献标识码**: A　　**文章编号**: 0253-4177(2004) 12-1612-06

2004-02-20 收到, 2004-07-24 定稿