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Schottky Barrier Characteristics of Polycrystalline and Epitaxial $CoSi_2$/n-Si(111) Contacts Formed by Solid State Reaction*

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Abstract: Polycrystalline and epitaxial $CoSi_2$ films are formed on the n-Si(111) substrates by solid state reaction of the as-deposited Co single-layer and Co/Ti bilayer with Si, respectively at different annealing phase. The $CoSi_2$/Si Schottky contacts are measured with the current-voltage and capacitance-voltage (I-V/C-V) techniques within the range of temperature from 90K to room temperature. The measured I-V characteristics have been analyzed with a model based on the inhomogeneity in Schottky barrier height, i. e., at high temperatures ($\geqslant\sim$ 200K) or low temperatures but with a large bias, the I-V curves can be described by using the thermionic emission theory with a Gaussian distributed barrier height over the whole junction, while at low temperatures and with a small bias, the current is dominated by some small patches with low barrier height. It results in a plateau-like section in the low temperature I-V curves around 10^{-7}A. At room temperature, the barrier height of polycrystalline $CoSi_2$/Si deduced from the I-V curve is about 0.57eV. For epitaxial $CoSi_2$, the barrier height depends on its final annealing temperature and increases from 0.54eV to 0.60eV with the annealing temperature increasing from 700℃ to 900℃.

Key words: Schottky barrier; silicide; I-V/C-V; inhomogeneity
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1 Introduction

Cobalt silicide ($CoSi_2$) is an important candidate of contacts and interconnects in modern very large scale integration (VLSI) technology due to its low resistivity, high thermal stability and no nucleation problems in narrow lines[1]. $CoSi_2$ has the same structure as CaF_2 with a small lattice mismatch with respect to Si, which makes the epitaxial growth of $CoSi_2$ on Si relatively easy. It is well known that appropriate heat treatment of Co/Ti bilayer on both (111) and (100) oriented Si results in an epitaxial $CoSi_2$ film (TIME: Ti-interlayer mediated epitaxial)[2], while the ex-situ annealing of a single Co layer on Si results in a polycrystalline silicide. Much research has been done on their formation mechanisms as well as the structural and electrical properties[2—6]. The Schottky barrier properties of a metal-semiconductor (M-S) contact are usually studied with current- and capacitance-voltage (I-V/C-V), photoemission spectroscopy and ballistics electron emission microscopy (BEEM). It is known that the

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Schottky barrier height (SBH) of a $CoSi_2$/Si contact depends on its formation parameters, such as growth type (solid state reaction, molecular beam epitaxy, ion implantation synthesis), annealing procedure, orientation, dopant concentration, etc[5—10]. The electrical properties of $CoSi_2$ films formed on the (100) oriented n-Si substrates by solid state reaction have been reported[7,8]. The epitaxial $CoSi_2$/Si(100) contacts have slightly lower SBH than the polycrystalline ones due to the Ti incorporation in the M-S interface, which also influences the barrier height distribution and the temperature coefficient. Both *I-V/C-V* and BEEM measurements have shown that MBE-grown $CoSi_2$(111)/Si(111) has a lower barrier height than $CoSi_2$(100)/Si(100)[9,10]. In this paper, the SBH properties of $CoSi_2$/Si (111) contacts formed by solid state reaction are studied by *I-V/C-V* from 90K to room temperature.

However, the charge carrier transport through a M-S junction is still to be defined. The forward *I-V* characteristics are commonly analyzed by using the thermionic emission (TE) theory with a uniform barrier height over the whole junction[11], however, which fails to describe the observed *I-V* results. Recently, the assumption that the barrier height is inhomogenous[12—14] has been confirmed by BEEM measurements[15]. By using a modified TE model with a Gaussian distributed barrier height over the whole junction, all the phenomena can be explained, including the different SBH deduced from different methods, non-linearity of the Richardson plot, strong dependence of both the apparent SBH and the ideality factor. However, it cannot explain the double threshold phenomenon that is sometimes observed in low-temperature *I-V* curves in the middle bias region and is attributed to the small patches of low barrier height. The *I-V* curves are well described over the whole temperature region with the combinative model of the Gaussian distribution model and the pinch-off one.

2 Experiment

The substrates used in this work were n^-/n^+ epitaxial Si (111) wafers (phosphor doped). The doping level of the epitaxial layer was about $8\times10^{15}cm^{-3}$ and the resistivity of the n^+ substrate was about $0.01\Omega\cdot cm$. After the thermal oxide layer of 300nm had been grown, the square windows in different sizes were opened with the standard lithography and wet etching procedures. Immediately after the standard RCA cleaning and dipping in a diluted HF solution to remove the native oxide on the active area, the wafers were loaded in a chamber of Oxford sputtering system with a base pressure of about 1×10^{-4}Pa. Titanium and cobalt were sequentially deposited without breaking the vacuum. The $CoSi_2$ silicidation was formed after a two-step ex-situ RTA (rapid thermal annealing) in the N_2 ambient with an interval of selective etching: first annealing at 600℃ for 1 min, then etching in a boiling solution of H_2SO_4 : H_2O_2 = 3 : 1 for 5min and in a boiling solution of NH_4OH : H_2O_2 : H_2O = 1 : 2 : 5 for 2min, finally annealing for 1 min at different temperatures (700, 800 or 900℃). An In-Ga alloy (liquid) was used as a backside ohmic contact.

The *I-V/C-V* measurements were carried out automatically with a computer controlled system composed of a Keithley 619 electrometer and a multi-frequency LCR HP 4274A meter. The diode was cooled down by liquid N_2 and the variation in the temperature is less than ±4K during the one-temperature-point measurements.

3 Results and Discussion

Forward *I-V* characteristics of an epitaxial $CoSi_2$/Si(111) at the temperature between 95K and 288K are displayed in Fig. 1. The $CoSi_2$ film is formed of Co(5nm)/Ti(3nm)/Si after the final annealing at 700℃ and the diode area is about $0.008cm^2$. Sheet resistance and XRD (X-ray

diffraction) measurements show that the epitaxial cobalt disilicide with low resistivity has been formed after annealing at 700℃ for 1min. With Rutherfold backscatting spectroscopy, the channeling minimum is obtained about 10%[2].

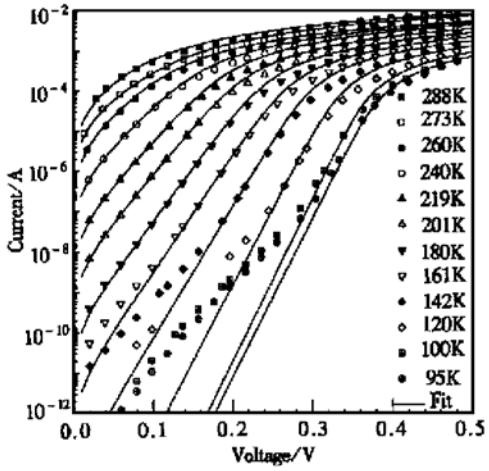

FIG. 1 Forward I-V Characteristics of Epitaxial $CoSi_2$ (111)/Si (111) Diode at Different Temperatures and Their Theoretical Fitting Curves Based on Modified TE Model

The forward I-V curves in Fig. 1 are analyzed with the expression based on the TE model[13]:

$$I = AA^{**}T^2\exp(-q\Phi^{I\text{-}V}/(kT)) \times \{\exp[q(V - IR_s)/(nkT)] - 1\} \quad (1)$$

where A is the diode area, A^{**} is the Richardson constant (for n-Si, $A^{**} = 112\text{A}\cdot\text{cm}^{-2}\cdot\text{K}^{-2}$), $\Phi^{I\text{-}V}$ and n are the apparent barrier height and the apparent ideality factor obtained from the forward I-V characteristics, R_s is the series resistance. The least square fitting is made with $\Phi^{I\text{-}V}$, n and R_s as adjustable parameters. The fitting curves are also shown in Fig. 1. At high temperatures or at low temperatures but with large bias, the fitting curves match the experimental data quite well. However, the deduced values of $\Phi^{I\text{-}V}$ and n are temperature dependent, especially at low temperatures. The phenomenon has been explained by using the barrier height distribution model[12, 13]. Assuming the barrier height over the whole junction is a Gaussian distribution, and the carrier transport through the different barrier height independently (parallel conductor model), the total current is given by an expression similar to Eq. 1 but with both $\Phi^{I\text{-}V}$ and n temperature-dependent[13]:

$$\Phi^{I\text{-}V} = \bar{\Phi} - \sigma_\Phi^2 q/(2kT) \quad (2)$$

$$1/n = (1 - \rho_1) + q\sigma_\Phi\rho_2/(kT) \quad (3)$$

where $\bar{\Phi}$ is the average barrier height and σ_Φ is the standard deviation. ρ_1 and ρ_2 are the bias coefficients of $\bar{\Phi}$ and σ_Φ, respectively. It implies that both plots of $\Phi^{I\text{-}V}$-$1/T$ and $1/n$-$1/T$ gives a straight line, which are shown in Fig. 2. The values obtained from the least square linear fitting of the experimental data are: $\bar{\Phi} = 0.58$eV, $\sigma_\Phi = 0.047$eV, $\rho_1 = -0.08$ and $\rho_2 = -0.05$, in agreement with the values reported[7, 13]. However, the linearity of both plots is not very good, which is attributed to the temperature dependence of both $\bar{\Phi}$ and σ_Φ, and the relatively large error of $\Phi^{I\text{-}V}$ and n due to the effect of the series resistance.

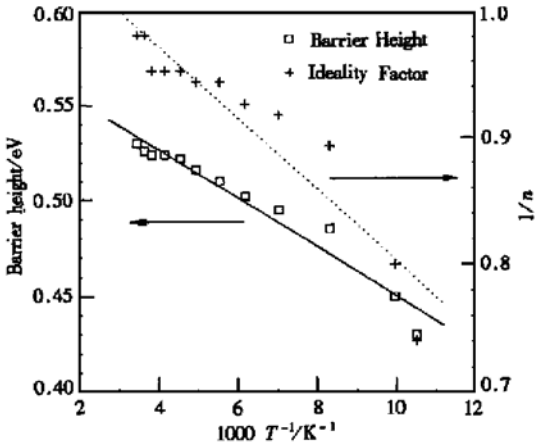

FIG. 2 Apparent Barrier Heights and Ideality Factors as a Function of Reciprocal Temperature and Their Linear Fittings

Figure 1 shows that there is a plateau-like section in the low temperature I-V curves around 10^{-7}A. Such double threshold behavior is attributed to the small patches with low barrier height. According to the pinch-off model, the current through the small patch can be expressed by[14]:

$$I_p = A_{eff}A^{**}T^2\exp(-q\Phi_{eff}/(kT)) \times \{\exp[q(V - I_pR_{sr})/(kT)] - 1\} \quad (4)$$

where Φ_{eff} and A_{eff} are the effective barrier height and the effective area of the patch, respectively. Both of them depend on the patch's parameter γ:

$$\gamma = 3(\Delta R_0^2/4)^{1/3} \quad (5)$$

where R_0 is the patch radius and Δ is the barrier height reduction at the M-S interface. R_{sr} is the series resistance of the patch, whose value is much larger than R_s due to the pinch-off effect around the patch. The total current is the sum of I_p and the current obtained from Eq. 1. Figure 3 shows the fitting curves with the parameters that $\gamma = 4.4 \times 10^{-4}\,cm^{2/3}V^{1/3}$ and $R_{sr} = 5 \times 10^5\,\Omega$. In the high bias region, the patch current is smaller than the current through the whole junction due to the large local series resistance of the patch. There exists a critical bias at which the patch current equals to the whole junction current. With the temperature increasing, the critical bias decreases. Above 180K, the patch current is negligible, and the I-V curves at the whole bias can be described by Eq. 1 alone.

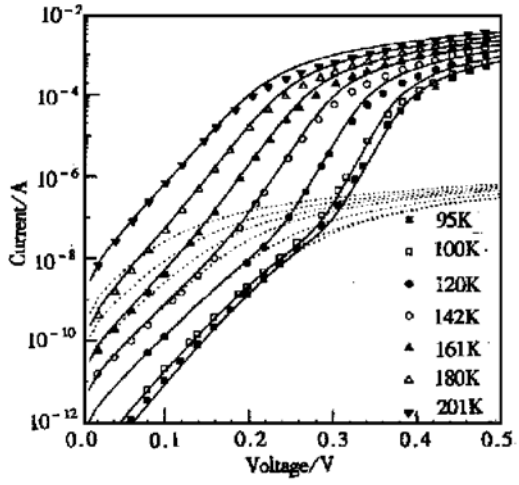

FIG. 3 Experimental and Theoretical I-V characteristics at Low Temperatures for Above Epitaxial CoSi (111)/Si (111) Diode The dotted curves show a patch current and the solid curves are the total current.

The diode has also been measured by C-V at the frequency of 100kHz and 500kHz. However, the plot of $1/C^2$-V_r deviates from the linearity significantly in the large reverse bias (V_r) region. The barrier height can only be deduced from the small reverse bias region, thus the deduced values of Φ^{C-V}, from 0.57 to 0.64eV, have a relatively large error. Taking the barrier height inhomogeneity into account, the results are in agreement with those deduced from I-V characteristics[12]. Moreover, the barrier height deduced from C-V increases slightly with the temperature decreasing. However, the relatively large experimental error of Φ^{C-V} makes it impossible to obtain a significative temperature coefficient of Φ^{C-V}.

The other two epitaxial $CoSi_2$/n-Si (111) diodes, formed by annealing for 1min at 800℃ and 900℃ respectively, have also been studied, with similar I-V and C-V characteristics obtained. The barrier height deduced from the room temperature I-V curve is about 0.54eV for the sample annealed at 800℃ and 0.60eV for the one annealed at 900℃. The C-V results also show the slight increase in the barrier height with the increase of the annealing temperature.

On the other hand, the barrier height of a polycrystalline $CoSi_2$/n-Si (111) diode is independent on its annealing temperature. The barrier height deduced from the room temperature I-V curve is about 0.57eV for both samples annealed at 800℃ and 900℃ respectively. The polycrystalline $CoSi_2$/Si diode of 0.008cm^2 in size will be analyzed in details below, which is formed by Co(20nm)/Si(111) with the final annealing at 800℃. Figure 4 (a) displays its forward I-V characteristics at temperatures from 92K to 291K. The theoretical fitting curves are the sum of two components: $I_{total} = I_{th} + I_{patch}$, where I_{th} is the current through the whole junction with a Gaussian distributed barrier height and I_{patch} is a patch current. Similar to the epitaxial $CoSi_2$/Si (111) diodes mentioned above, the experimental I-V characteristics at the whole bias can be fitted over the whole temperature region. In the small bias region and at low temperatures, the patch current dominates. The patch parameter deduced

from the fitting is: $\gamma = 4.05 \times 10^{-4}\,\mathrm{cm}^{2/3}\,\mathrm{V}^{1/3}$. At high temperatures or in the large bias region but at low temperatures, the current through the whole junction dominates. The apparent barrier height and the apparent ideality factor are displayed in Fig. 4 (b) as a function of the reciprocal temperature. From the least square linear fitting of both plots of $\Phi^{I\text{-}V}$–$1/T$ and $1/n$–$1/T$, the mean of barrier height, the standard deviation and their bias coefficients are obtained as: $\bar{\Phi} = 0.69\mathrm{eV}$, $\sigma_\Phi = 0.07\mathrm{eV}$, $\rho_1 = -0.2$ and $\rho_2 = -0.06$, respectively.

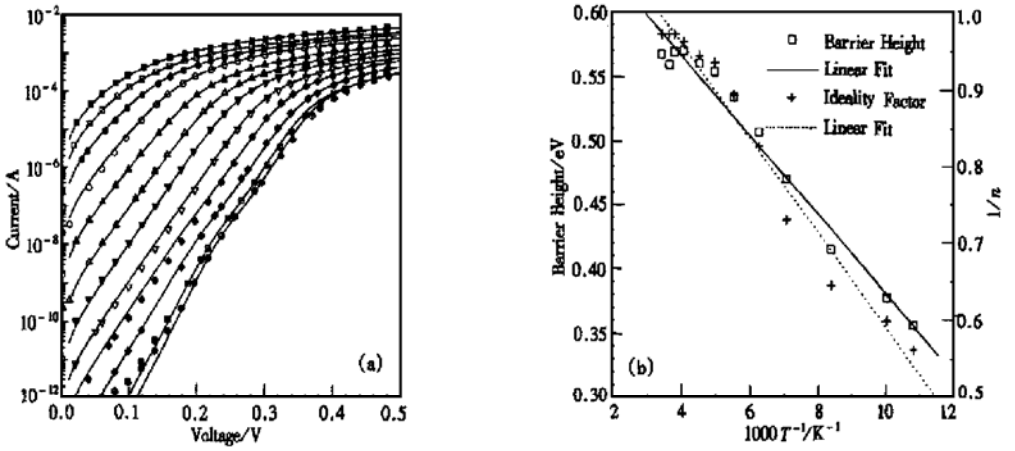

FIG. 4 Results of Polycrystalline $CoSi_2$/Si(111) Diode (a) Forward Experimental I–V Characteristics (Symbols) and Calculated Ones (Solid Curves); (b) Apparent Barrier Heights and Ideality Factors as a Function of Reciprocal Temperature and Their Linear Fittings

The barrier height of the epitaxial $CoSi_2$/Si (111) diodes is slightly lower than that of the polycrystalline ones. Similar phenomenon is also observed for the $CoSi_2$/Si(100) diodes. It can been attributed to the Ti incorporation in the $CoSi_2$–Si contact during the TIME process[7]. It is known that Ti/Si or $TiSi_2$/Si contact has a lower barrier height than $CoSi_2$/Si contact[16]. With the annealing temperature of the Co/Ti/Si system increasing, the Ti concentration in the $CoSi_2$/Si interface is reduced, thus the barrier height increases slightly. Compared with our previous study on $CoSi_2$/Si (100) diodes[7,8], the barrier height of $CoSi_2$/Si (111) is lower than that of $CoSi_2$/Si(100) diodes. It reveals that the barrier height depends on the orientation of the $CoSi_2$ structure, which is in agreement with the I–V measurements on the MBE growth $CoSi_2$/Si diodes reported by Jimenez *et al.*[9] and the BEEM measurements reported by Sirringhaus *et al.*[10].

4 Conclusion

The forward I–V characteristics of both polycrystalline and epitaxial $CoSi_2$/Si(111) diodes are analyzed by using the combined model of the Gaussian distribution model with the barrier heights over the whole junction and the pinch-off model with the low barrier height patch. The epitaxial $CoSi_2$(111)/Si(111) has a lower barrier height than the polycrystalline ones. It is attributed to the Ti incorporation into the $CoSi_2$–Si interface during the solid state reaction of the Co/Ti/Si system as well as the dependence of the barrier height on the orientation of the $CoSi_2$ layer. The $CoSi_2$(111)/Si(111) contact has a lower barrier height than other orientations on Si substrate.

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固相反应制备的多晶和外延 $CoSi_2$/n-Si(111) 接触的肖特基特性*

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摘要: 通过硅 (111) 衬底淀积的单层 Co 或 Co/Ti 双金属层在不同退火温度的固相反应, 在硅上形成制备了多晶和外延 $CoSi_2$ 薄膜. 用电流-电压和电容-电压 (I-V/C-V) 技术在 90K 到室温的温度范围内测量了 $CoSi_2$/Si 肖特基接触特性。用肖特基势垒不均匀模型分析了所测得的 I-V 特性, 在较高温度下 (≥~ 200K) 或较低温度的较大偏压区域, I-V 曲线能用热激发和在整个结面积上势垒高度的高斯分布模型描述. 而在较低温度的较小偏压区域, 电流由流过一些小势垒高度微区的电流决定, 从而在低温 I-V 曲线上在约 10^{-7}A 处有一个 "曲折". 在室温下, 从 I-V 曲线得到的多晶 $CoSi_2$/Si 的势垒高度为约 0.57eV. 对外延 $CoSi_2$, 势垒高度依赖于最后退火温度, 当退火温度从 700℃升到 900℃, 势垒高度从 0.54eV 升高到 0.60eV.

关键词: 肖特基势垒; 硅化物; I-V/C-V; 不均匀性

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