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The Jitter Performance Comparison Between DLL and PLL-Based RF CMOS Oscillators

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Abstract: By jitter performance comparison between PLL (Phase Locked Loop) and DLL (Delay Locked Loop), a helpful equation is derived for the structure choice between DLL and PLL-based synthesizers fabricated in CMOS processes to get an optimum jitter performance and power consumption. For a frequency synthesizer, a large multiple factor prefers PLL-based configuration which consumes less power, while a small one needs DLL-based topology which produces a better jitter performance.

Key words: Jitter; PLL; DLL; frequency synthesizer; RF CMOS transceiver; Local Oscillator (LO); Voltage Controlled Delay Line (VCDL); VCO

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1 Introduction

Growth in demand of wireless communications has driven recent efforts to dramatically increase integration levels in RF transceivers. One approach is to implement all the RF functions in a single chip with CMOS technology[1], which is developing rapidly and makes monolithic RF CMOS transceiver reasonable.

Oscillators made by PLL (Phase Locked Loop) synthesizers are important to shift down a received carrier signal spectrum to a lower frequency in a transceiver as Local Oscillators (LO), or shift a signal spectrum up to a higher frequency band in the case of a transmitter. A lot of difficulties in the tradeoff in the design of PLLs make it very hard to fabricate a RF CMOS oscillator with good jitter performance; A close relative of PLL synthesizer is DLL (Delay Locked Loop)-based synthesizer, in which a Voltage Controlled Delay Line (VCDL) is used to replace of a Voltage Controved Oscillator (VCO) in a PLL[2,3]. The VCDL usually consists of a cascade of k identical gain stages with variable delay. So this kind of DLL provides precisely spaced timing edges even in the presence of temperature and process variations. This character can be used to synthesize multiple of the input frequency, which is performed by the edge combining. In this case, the jitter accumulated by the end of the delay chain does not contribute to the starting point of the next cycle since the delay chain is not configured as an oscillator. The reference determines the next transition point instead. This kind of system has superior jitter performance than that of a PLL system.

In most clock synthesis applications, a VCO is locked to a low-jitter reference, often in the form of a crystal. Most of the output jitter results from noise sources in the phase detector, loop filter, and VCO. With a careful PLL design, the jitter in the VCO is usually the dominant contributor[4]. The

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ring-oscillator VCO is a popular choice in many applications. The jitter cycle of oscillation is determined by the sum of the timing error contributions of each inverter stage in the ring[5]. With each cycle of oscillation the jitter variance, relative to a reference transition in the past continues to grow, unless the oscillator is configured in a PLL. In a ring-oscillator PLL oscillator, however, the total timing jitter is made up of the errors in the most recent cycles of oscillation, yet to be corrected by the PLL, and therefore improves for higher loop bandwidth.

This paper tries to compare the timing jitter performances of DLL and PLL-based RF oscillators. Section 2 is the jitter performance comparison between DLL and PLL-based oscillators; Section 3 gets the conclusions from the analysis and comparison in sections above.

2 Jitter Comparison

Timing jitter in a ring-oscillator PLL depends on the interaction of noise in the oscillator with the dynamics of the phase-locked loop. It has shown in Reference[5] that the timing jitter variance at the end of a chain of inverters is given by the sum of the contributions of each stage. If each stage contributes a timing error with variance $\overline{\Delta t_n^2}$, then the total jitter at the end of N stages is $N\ \overline{\Delta t_n^2}$. The subscript "n" indicates "noise". In a ring-oscillator, this timing error determines the starting point of the next cycle and therefore creates a permanent phase shift in the output signal. However, if the ring-oscillator is configured in a phase-locked loop, the phase difference between the reference clock and the oscillator output is detected and compensated for by the dynamics of the loop. The phase detector will sense the shift and create an error signal to change the frequency of the ring-oscillator VCO in a way that moves the phase of output in the right direction.

Since the amount of phase adjustment is usually small, the phase error is not corrected in one clock cycle, but it is reduced gradually over the course of several cycles. Depending on the bandwidth of the loop filter in the PLL, the phase error may remain for up to several hundreds of cycles. Analysis of the accumulated phase jitter and its relation to the loop bandwidth is important for PLL synthesizers. In most PLL clock synthesizer designs, the reference clock comes from a very low jitter source such as crystal oscillator. Therefore, the jitter in the ring-oscillator is the main source of the phase error in the synthesized signal. In this case the bandwidth of the loop filter determines how large the accumulated timing jitter gets. In Reference[4], the rms phase jitters is given by Eq (1):

$$\sqrt{E[\Theta_{\mathrm{tot}}^2(nT_{\mathrm{in}})]} \approx \sqrt{\frac{1}{2\epsilon}} \times \frac{2\pi\Delta\tau_{\mathrm{rms}}}{T_{\mathrm{in}}} = \alpha\frac{2\pi\Delta\tau_{\mathrm{rms}}}{T_{\mathrm{in}}} \tag{1}$$

where $\Delta\tau_{\mathrm{rms}}$ is rms of the total delay of the delay chain, T_{in} is the peroid of the input, and $\alpha = 1/\sqrt{2K_{\mathrm{d}}K_{\omega}aT_{\mathrm{in}}}$ is defined as the accumulation factor. Here, K_{d} and K_{w} are the gains of the phase detector and the VCO, and a equals to the R in value in the filter of the charge pump. From the result, the rms timing jitter in a PLL is seen to be α times larger than the intrinsic jitter in the delay chain. The accumulation factor α is inversely proportional to the square root of $K_{\mathrm{d}}K_{\omega}aT_{\mathrm{in}}$. When stability requirements are met, the jitter accumulation factor can be lowered by increasing the bandwidth of the loop filter, $\omega_{\mathrm{L}} = K_{\mathrm{d}}K_{\omega}a$.

In a DLL, phase jitter is not passed on from one period of the clock to the next since the output of the delay-line is not fed back to the input. Therefore, we expect the jitter in a DLL to be much smaller than that in a ring-oscillator based PLL. In Reference[4], the rms output jitter is given by Eq(2):

$$\sqrt{E[\Theta_{\mathrm{tot}}^2(nT_{\mathrm{in}})]} = \frac{2\pi\Delta\tau_{\mathrm{rms}}}{T_{\mathrm{in}}} \tag{2}$$

This expression is similar to the result for the PLL, given in Eq(1), except that there is no noise enhancement factor α. Therefore, a DLL provides superior timing jitter performance. How much better depends on the size of α.

Supposing that $f_{out} = Nf_{in}$, where f_{out} is the output of the local oscillator; f_{in} is the reference frequency; N is the multiple factor. We realize this oscillator respectively by PLL and DLL-based synthesizers and compare their jitter performances.

First, with a PLL-based synthesizer, the derived ring-oscillator jitter result is valid if K_d is replaced by K_d/N. Then we get rms phase jitter as Eq(3):

$$\sqrt{E[\Theta_{tot}^2(nT_{in})]_{N,P}} = \sqrt{N}\alpha\frac{2\pi\Delta\tau_{rms}}{T_{in}} \quad (3)$$

where subscript N denotes the multiple factor, subscript P denotes PLL. In ring-oscillators, power is minimized by using fewest delay stages needed. Assuming the number of the delay units in the ring-oscillator is m (m is an integer within 3 to 5) and the variance of jitter per stage is $\Delta\tau_{rms,1}$, total jitter variance is $m\Delta\tau_{rms,1}$. Eq(3) can be rewritten as

$$\sqrt{E[\Theta_{tot}^2(nT_{in})]_{N,P}} = \sqrt{N}\alpha\frac{m2\pi\Delta\tau_{rms,1}}{T_{in}} \quad (4)$$

When the oscillator is realized with a DLL-based synthesizer, the conclusion of the rms jitter of a DLL derived above in Eq(2) can be used directly. Because the multiple factor is N, as we introduced above, there should be N stages in the delay line in a DLL-based synthesizer to generate the high frequency signal. Assuming that the same delay unit as that in VCO above is used in the delay chain, namely, the variance of jitter of per stage is also $\Delta\tau_{rms,1}$, total jitter variance of the delay line equals to $N\Delta\tau_{rms,1}$. Eq(2) can be rewritten as

$$\sqrt{E[\Theta_{tot}^2(nT_{in})]_{N,D}} = \frac{2\pi\Delta\tau_{rms}}{T_{in}} = N\frac{2\pi\Delta\tau_{rms,1}}{T_{in}} \quad (5)$$

where subscript N denotes the multiple factor, subscript D denotes DLL.

By comparing Eq.(4) to Eq.(5), we get a comparison factor h:

$$h = \frac{\sqrt{E[\Theta_{tot}^2(nT_{in})]_{N,P}}}{\sqrt{E[\Theta_{tot}^2(nT_{in})]_{N,D}}} = \frac{\sqrt{N}\alpha\frac{2\pi m\Delta\tau_{rms,1}}{T_{in}}}{N\frac{2\pi\Delta\tau_{rms,1}}{T_{in}}} = \frac{\alpha m}{\sqrt{N}} \quad (6)$$

In practice, α is about several decades in value, m is within 3 to 5. For example, $\alpha = 25$ and $m = 5$, if the comparison factor is 1, then $N = 15625$, which means, in this case, only a delay chain with 15625 units can produce the same jitter that a ring-oscillator PLL-based synthesizer with $\alpha = 25$ and $m = 5$ does. From this analysis, how much the great performance enhancement that a DLL over a PLL can be found clearly.

When $f_{in} = 40\text{MHz}$, $f_{out} = 1\text{GHz}$ (1GHz is in the band of mobile communications), $N = 25$, so $h = 25$, the jitter can be improved 25 times by using a DLL-based synthesizer; When $f_{in} = 0.2\text{MHz}$, $f_{out} = 1\text{GHz}$ then $N = 5000$, so $h = 1.8$, the relatively low h means that when the N is very large in a high resolution synthesizer, for example, the DLL-based synthesizer can not perform as much better as we expected and what worse, however, the long VCDL chain which the large N needed consumes much more power, and this makes it not reasonable for a high resolution synthesizer.

3 Conclusions

In this paper, the jitter performances of DLL and PLL-based synthesizer as well as the jitter comparison between them were performed. From the comparison we found that the DLL-based synthesizer has good jitter performance over the PLL-based topology, but it is not always a good choice to fabricate a CMOS RF local oscillator by DLL-based synthesizer. To a high resolution oscillator in which the channel spacing is small(200KHz), such as AMPS, only a little jitter character enhancement is achieved at the cost of larger power that a long delay chain consumes. We derived a practical equation —— Eq.(6) for the choice between PLL and DLL-based synthesizers. The higher the h is, the higher the jitter quality will be. This is what we expected for a DLL-based synthesizer.

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对基于 DLL 和 PLL 的射频 CMOS 振荡器的相位抖动比较

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摘要: 通过对 PLL 和 DLL 相位抖动的比较, 结合 DLL 倍频器的结构特点, 得出了一个有用的公式, 这个公式可以用于在 PLL 和 DLL 两种结构中选择出一个最佳方案, 使得在使用 CMOS 工艺实现频率合成器时能够得到最佳的功耗和相位抖动的折衷. 对于倍频系数很大的倍频器宜采用基于 PLL 的结构, 这样可以消耗较少的功率; 而对于较小的倍频系数的倍频器要采用基于 DLL 的结构, 这样相位抖动特性将非常优良.

关键词: 相位抖动; PLL; 延时锁相环; 频率合成器; 射频 CMOS 收发器; 本振; 压控延时线; 压控振荡器

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