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A Novel High-Voltage Detector Integrated into SPIC by Using FFLR*

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Abstract: A novel high-voltage detector that can be integrated into SPIC (Smart Power IC) is proposed. The structure is designed on the basis of normal junction terminal technique of FFLR (Floating Field Limiting Rings) system. The field-limiting ring as a voltage divider, is used to optimize the surface field. The voltage of main junction increases from 0 to a high value, while the utmost ring is designed to vary within a small range, which can be handled by using low voltage logic circuits. An example of 400V rings system is analyzed and simulated for this structure. The results prove that the high voltage detector can detect high voltage in SPIC. The structure can be integrated into SPIC. Besides, it is compatible with CMOS or BCD(Bipolar CMOS Dmos) technology, without any additional processes required.

Key words: FFLR; high voltage detector; voltage divider; detector ring
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1 Introduction

Smart Power IC (SPIC) combines the power device with CMOS logic and/or bipolar analog circuits on one chip. The integration of discrete elements makes significant improvement in performance at a lower cost. Furthermore, SPIC's logic circuit involves the regulations of over-current, over-voltage and over-temperature conditions[1]. However, the over-voltage protection is designed only for low voltage circuits. No report has been found on that for a high voltage circuit, especially for the high voltage circuits of a power device integrated in SPIC. If a high voltage signal is directly transmitted to a low voltage circuit, the low voltage circuit will break down. So a high voltage detector is important to symbolize the high voltage, with which low voltage circuits can be handled. The normal detector for high voltage consists of two series resistance as a voltage divider. The upper resistance should be large enough to get a low power loss. However, it is difficult not only to integrate the large resistance into IC, but also to handle the value of the resistance accurately in the normal IC processing. That is why the over-voltage protection circuit can not be integrated in SPIC. A new way has been proposed to detect the high voltage in this paper.

Since the SPIC has high voltage circuits or high voltage devices. the junction terminal technology is often used to improve the surface break-

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down voltage. The FFLR (Floating Field Limiting Rings) as a voltage divider[2—3], is very useful to increase the breakdown voltage of the junction terminal. Tang[4] has discussed the single ring's design, but the results cannot be used in the multiple rings system directly. No discussion has been made on how to design a FFLR in SPIC or power devices for some purpose, i. e. to make the utmost ring acts as a voltage detector. It is found that if more rings are added to the outer of the normal ring system, the utmost ring near the boundary of depletion region can be designed as a high voltage detector, as shown in Fig. 1. This high voltage detector's voltage, which is low enough for low-voltage circuits to handle and is connected to the logic circuits, can drive the protection circuits for SPIC or power devices. This high voltage detector can also be integrated into SPIC. That is to say, the integrated high voltage detector would make the SPIC smarter than before.

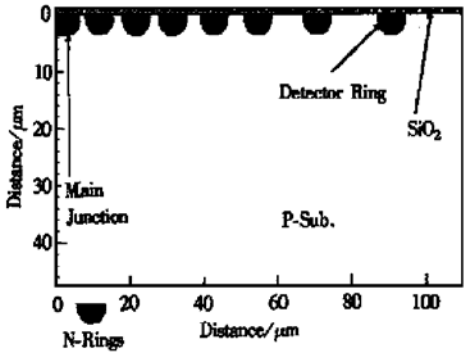

FIG. 1　Structure of the Rings System with High-Voltage Detector

2　Theory

The first paper on field limiting rings informed that the rings on surface could act as voltage dividers[2]. To design a high voltage detector, firstly, the normal FFLRs should be designed to increase surface breakdown voltage, and then the location of the detector be confirmed. In this way, the normal FFLRs were designed and the equation of the voltage of the rings versus that of the main junction of FFLR system was deduced[5]:

$$V_{i,i+1} = 4\left(\frac{N_B}{10^{16}}\right) r_i^2 \ln\left(1 + \frac{4}{r_i\left(\frac{N_B}{10^{16}}\right)^{0.94}}\right) + 16\left(\frac{N_B}{10^{16}}\right)^{0.06} r_i\left[\ln\left(1 + \frac{4}{r_i\left(\frac{N_B}{10^{16}}\right)^{0.94}}\right) - 1\right] \quad (1)$$

where V_i, in V, stands for the voltage of ring i; r_i, in μm, stands for the curvature radius of ring i; N_B, in cm^{-3}, stands for the substrate doping level. In normal design, even the utmost ring has a higher voltage up to about 100V[6], which can cause the breakdown of the low voltage logic circuit. Thus, to design a voltage detector, more rings are needed to be added to the outside of the normal ring system to divide the 100V voltage. The voltage can be divided into several volts. If the voltage of a ring is designed to be low enough about 10V, it can act as a high voltage detector, with which the logic circuits can be handled. And the location of the detector can be calculated according to the equation[7]:

$$X_d = \sqrt{\frac{2V\epsilon_s}{qN_B}} = \sqrt{\frac{2 \times 10\epsilon_s}{qN_B}} = \sqrt{\frac{1.28 \times 10^8}{N_B}} \quad (2)$$

X_d is the distance of the detector ring's outside from the depletion boundary of FFLR when the main junction's voltage rises up to the breakdown voltage. X_d is in μm; N_B is the same as before. So, the detector ring is chosen to near the boundary of depletion with the distance X_d, as shown in Fig. 2. It is important to point out that the utmost ring

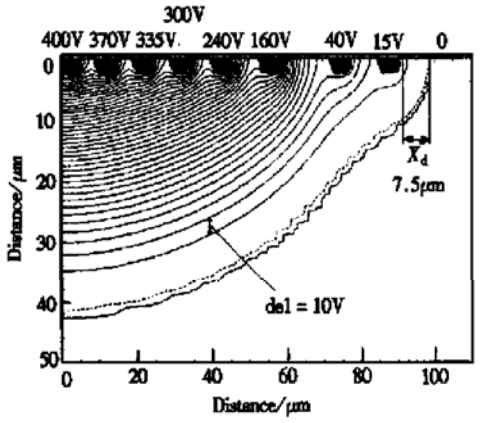

FIG. 2　Potential Contour　The difference between two adjacent lines is 10V.

can only be connected to a capacitance, such as the gate of a MOST. If the ring is directly connected to a resistance, the breakdown voltage will decrease a lot.

3 Simulation

Here is an example of the high voltage detector, with the structure's cross-section shown in Fig. 1. This structure is simulated by using TMA's MEDICI[8]. Parameters of the structure are as follows: the breakdown voltage is about 410V; substrate is p-type with the doping level of 3×10^{14} cm^{-3}; the surface concentrate of rings is 5×10^{18} cm^{-3}; the junction depth is 3.5μm and the interface charge is $1\times10^{10}cm^{-2}$(The interface charge is used as a statement added in the MEDICI programs[9]). There are seven n-type rings in the structure. The inner five rings are designed to increase the surface breakdown voltage form the equation (1)[4]. The two outer rings are the added rings designed to detect the voltage of the main junction. The utmost ring is designed to be a voltage detector. The X_d is about 6.5μm from equation (2). The detector ring's outside is chosen to be 7.5μm from the boundary of depletion region in Fig. 2, which is larger than the calculated value, so the highest voltage of the detector is about 15V. Figure 3 shows the linear relationship between the voltages of all rings and that of the main junction, which approximates to the experimental result of Whight[6]. The voltage of the voltage detector (the outmost ring) begins to increase when the voltage of the main junction increases up to 270V. Figure 4, as a selective enlargement of Fig. 3, shows clearly that the voltage of the main junction is in one to one correspondence with that of the detector. In Fig. 4, point A (the cross point) in the line is the protection point in this simulation. The detector ring's voltage is over 3V, and the corresponding main junction's voltage is about 310V.

The detector ring is connected to a NMOS's gate of the logic circuits. The voltage of the ring

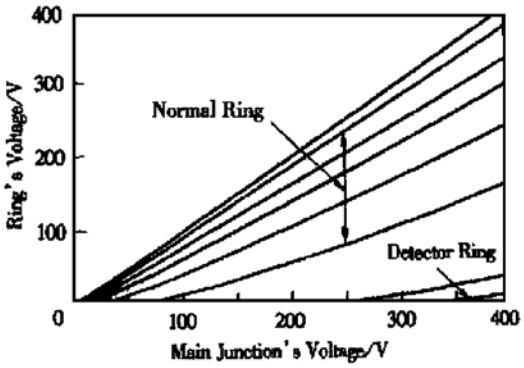

FIG. 3 Voltage of Ring Versus that of the Main Junction

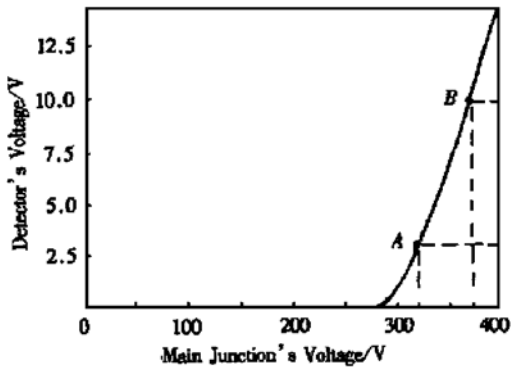

FIG. 4 Voltage of Detector Versus that of the Main Junction

can be transmitted to a NMOS's gate directly in this design. This can be explained in this way: when the voltage of the main junction increases up to 310V, that of the detector ring will increase up to over 3V, which can be transmitted to the gate of NMOS in logic circuits. The threshold voltage of the NMOS is 3V, so the voltage is a little higher than the threshold voltage of the NMOS, and the protection circuit begins to work. The adjustment of threshold voltage can be designed in the same process of the power device. MEDICI's circuit simulation has proved that when the voltage of the detector increases to over 3V, the NMOS begins to work. A MEDICI circuit simulation[8] has been done to prove the detector's availability: the detector is connected to the gate of a NMOS. The parameters of NMOS are as follows: V_t is 3V; the gate width is 3μm; the gate length is 3μm. The

NMOS can work at the voltage of detector a little higher than 3V. For example, if a higher voltage of the main junction point B about 370V needs protection, and the voltage of the detector is 10V, i.e., the voltage of the detector is much higher than the threshold voltage of the normal NMOS, the detect ring can be connected to an input pin of a CMOS comparator[10] of low voltage circuits. The protection voltage can be designed in the circuit design.

The additional rings can be done in a normal rings process, without any additional processes required nor having to change the CMOS or BCD (Bipdlar CMOS Dmos) technology.

4 Conclusion

A novel high voltage detector is introduced in this paper. The ring system acts as a voltage divider. Two more rings are added to the outer of a normal rings system and the utmost ring is designed to be a high voltage detector near the boundary of the depletion region of normal FFLR. Both the analysis and simulation prove that the structure can detect the high voltage in SPIC effectively and can be integrated in SPIC. This structure is compatible with the CMOS or BCD technology and can be used in SPIC, HVIC(High Voltage IC) and Power devices.

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一种新型的用浮空场限环实现的可集成在 SPIC 中的高压电压探测器*

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摘要: 提出一种可以集成在 SPIC(智能功率集成电路) 内部的高压电压探测器的方法, 其理论是基于基本的结终端技术中的浮空场限环系统, 把场限环系统作为表面电压分压器. 在通常的场限环外侧再增加两个环, 对外侧环电压再一次分压, 并把最外侧环设计成高压电压探测器. 这样当主结电压上升到一个高压时, 最外侧的环可以只有几伏到十几伏的变化, 这样环(探测器) 上的信号既可以表征主结高电压, 又可以由低压逻辑电路处理. 以一个 400V 的结构为例, 分析并模拟了这个结构. 结果证明可以有效探测 SPIC 的高压并可以集成在 SPIC 中. 同时, 该结构可以与 CMOS 和 BCD 工艺兼容, 且工艺上也不会增加步骤.

关键词: 浮空场限环; 高压电压探测器; 分压器; 探测环

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