第 21 卷第 4 期　　半　导　体　学　报　　Vol. 21, No. 4
2000 年 4 月　　CHINESE JOURNAL OF SEMICONDUCTORS　　Apr., 2000

A Novel Ultra-Thin Channel Poly-Si TFT Technology

ZHANG Sheng-dong(张盛东), HAN Ru-qi(韩汝琦), GUAN Xu-dong(关旭东), LIU Xiao-yan(刘晓彦) and WANG Yang-yuan(王阳元)

(*Institute of Microelectronics, Peking University, Beijing* 100871, *China*)

Abstract: A novel low temperature poly-Si(LTPS) ultra-thin channel thin film transistor (UTC-TFT) technology is proposed. The UTC-TFT has an ultra-thin channel region (30nm) and a thick drain/source region (300nm). The ultra-thin channel region that can result in a lower grain-boundary trap density in the channel is connected to the heavily-doped thick drain/source region through a lightly-doped overlapped region. The overlapped lightly-doped region provides an effective way for the electric field to spread in the channel near the drain at high drain biases, thereby reducing the electric field there significantly. Simulation results show the UTC-TFT experiences a 50% reduction in peak lateral electric field compared to that of the conventional TFT. With the low grain-boundary trap density and low drain electric field, excellent current saturation characteristics and high drain breakdown voltage are achieved in the UTC-TFT. Moreover, this technology provides the complementary LTPS-TFTs with more than 2 times increase in on-current, 3.5 times reduction in off-current compared to the conventional thick channel LTPS TFTs.

Key words: TFT; poly-silicon; kink-effect; ultra-thin channel
PACC: 2560S; 2570F; 7260
CLC number: TN321^{+}.5　**Document code**: A　**Article ID**: 0253-4177(2000)04-0317-08

多晶硅超薄沟道薄膜晶体管研制

张盛东　韩汝琦　关旭东　刘晓彦　王阳元

(北京大学微电子学研究所, 北京　100871)

ZHANG Sheng-dong(张盛东) was born in 1964. He is presently a Ph. D candidate. His research areas are the physics, structures and technologies of novel semiconductor device.

HAN Ru-qi(韩汝琦) was born in 1938. He is currently of professor. His research areas lie in the nanoscale semiconductor devices physics, modeling and structures.

GUAN Xu-dong(关旭东) was born in 1939. He is currently a professor. His research areas are the nanoscale semiconductor devices physics, structures and technologies.

LIU Xiao-yan(刘晓彦) was born in 1966. She is currently an associate professor. She is engaged in research work on the nanoscale semiconductor devices physics and modeling.

WANG Yang-yuan(王阳元) was born in 1935. He is an academician of Chinese Academy of Sciences. His main research areas lie in SOI devices and circuits.

Received 26 September 1999, revised manuscript received 14 December 1999

摘要: 提出了一种新结构的低温多晶硅薄膜晶体管(poly-Si TFT). 该 poly-Si TFT 由一超薄的沟道区和厚的源漏区组成. 超薄沟道区可有效降低沟道内陷阱密度, 而厚源漏区能保证良好的源漏接触和低的寄生电阻. 沟道区和源漏区通过一低掺杂的交叠区相连接. 该交叠区使得在较高偏置时, 靠近漏端的沟道区电力线能充分发散, 导致电场峰值显著降低. 模拟结果显示该 TFT 漏电场峰值仅是常规 TFT 的一半. 实验结果表明该 TFT 能获得好的电流饱和特性和高的击穿电压. 而且, 与常规器件相比, 该 TFT 的通态电流增加了两倍, 而最小关态电流减少了 3.5 倍.

关键词: 薄膜晶体管; 多晶硅; kink 效应; 超薄沟道
EEACC: 2560S; 2570; 7260
文章编号: 0253-4177(2000)04-0317-08

1 Introduction

As well known to us, low temperature poly-Si(LTPS) TFT has much higher effective carrier mobility than amorphous silicon TFT (a-Si TFT)[1—3]. So, LTPS TFT is expected to be one of the most promising technologies of building fully-integrated AMLCD system on glass[1]. The research so far has been focused on the realization of digital circuits on glass[4,5]. However, analog functionality must also be included in the data driving scheme in order to achieve the grey scale or full-color images[6,7]. The basic building block for the analog circuits is an operational amplifier. Due to the poor saturation and low on-current characteristics of LTPS TFTs, it is extremely difficult to implement to operational amplifier with useful voltage gain and bandwidth. Moreover, the low on-current in the LTPS TFTs prevents the digital circuits on glass from meeting the speed and driving requirements for the high resolution displays. For a high on-current, TFTs with ultra-thin film have been investigated[8,9]. However, these devices are of poor drain/source contact, large series resistance and low drain breakdown. For good saturation characteristics, the Elevated Channel TFT (ECTFT) technology has been proposed[10] but fails to provide the ultra-thin film devices. On the other hand, short channel poly-Si devices are considered more suitable for the high-speed digital circuit applications[6,11]. Unfortunately, the devices with conventional technology have a low drain breakdown voltage that cannot satisfy the digital circuits driving requirement. In this paper, a novel Ultra-Thin Channel TFT (UTC-TFT) technology is proposed. Experimental results show that this technology provides LTPS TFT devices with excellent saturation characteristics, much increased drain breakdown voltage, high current driving capability, and low leakage current, which are very useful in fully-integrated high resolution and full-color AMLCD system on glass.

2 Device Structure Analysis

It is known that the poor saturation characteristics in LTPS-TFTs limit severely the application of TFT devices for analog circuits, with those in poly-Si TFTs being revealed

to arise with a similar mechanism to that for the kink effect in SOI MOSFETs, that is to say, the channel avalanche multiplication occurrs in the high-field region near the drain, which is combined with the floating body of the device[12]. However, in poly-Si TFTs, there is an additional mechanism related to the high grain-boundary trap density that exaggerates the effect of avalanche multiplication further[13]. So, both the high electric field at the drain and high grain-boundary trap density in the channel should be reduced effectively in order to obtain excellent current saturation characteristics in LTPS-TFTs. Due to the reasons above, a novel UTC-TFT technology is proposed.

The schematic cross-section of the n-channel UTC-TFT is shown in Fig. 1. The device has an ultra-thin channel region (30nm) and a thick drain/source region (300nm). It has been reported in the earlier work[8] that the LTPS film with the thickness more than 20nm has a nearly constant grain-boundary trap concentration. It means that the trap density in that LTPS film is proportional to the LTPS film thickness approximately. Here, the trap density is defined as the ratio of the total traps in the channel to the channel area, hence the ultra-thin LTPS film (20nm—30nm) has a low trap density. The ultra-thin LTPS film can also improve the I-V characteristics of LTPS-TFT, as will be presented in Section 4 of this paper.

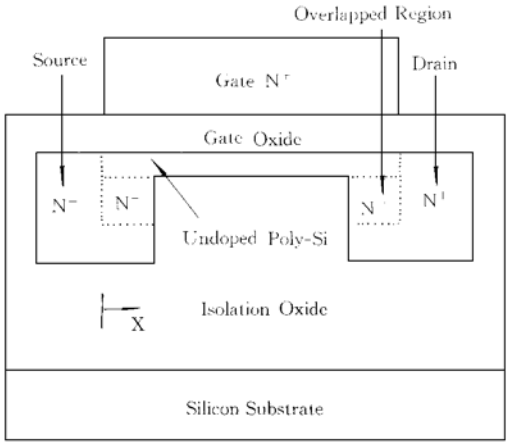

FIG. 1　Schematic Cross-Section of n-Channel UTC-TFT

Another unique feature of the UC-TFT structure is that the undoped ultra-thin channel region is connected to a heavily-doped thick drain/source region through a lightly-doped overlapped region, which is identical with a conventional lightly doped drain (LDD)[14], and equivalently leads to a much-increased drain junction depth[11]. At high drain biases, it provides an effective way for the electric field to spread in the channel near the drain, thereby reduces the lateral electric field there significantly. At the same time, the thick drain/source region is also used to obtain good drain/source contacts and reduce the series resistance. In order to calculate how much the drain electric field is reduced in the UTC-TFT compared with that in the conventional LTPS-TFT devices, a 2-dimensional simulator MEDICI[15] was used. MEDICI uses 2-D numerical simulator for device analyses. For the sake of simplicity, the single crystalline silicon model obtained in MEDICI was employed to estimate the electric field in LTPS-TFTs. Besides the UTC-TFT, the conventional TFT and ECTFT are also simulated for comparison. In the simulation, the conventional drift-diffusion model, the local impact-ionization model and the parameters

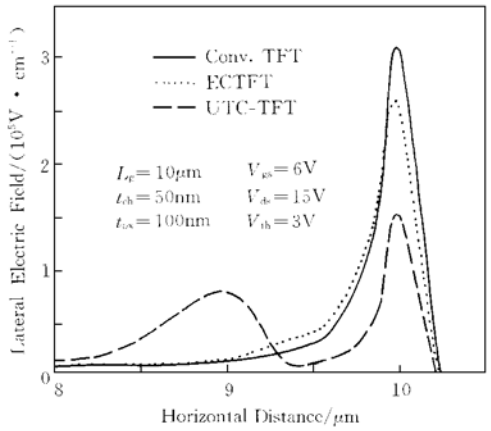

FIG. 2 Simulated Electric Field Distribution Along the Channel/Drain Junction Region for Various TFTs

regarding the nature of LTPS material were used. Figure 2 shows the simulated lateral electric field distribution near the drain/channel region for conventional TFT, ECTFT and UTC-TFT. Where, L_g, t_{ch} and t_{ox} are the gate length, channel thickness and gate oxide thickness of TFT, respectively. And V_{gs}, V_{ds} and V_{th} are the gate-source voltage, drain-source voltage and threshold voltage, respectively. It can be seen the peak value of lateral electrical field in the UTC-TFT is only 50% of that in the conventional TFT, and 65% of that in the EFTFT. With the much-reduced electrical field and grain-boundary trap density in the channel near the drain, good current saturation and high drain breakdown voltage in UTC-TFT are expected.

3 Device Fabrication

The complementary UTC-TFT devices have been fabricated in a simple low temperature process (≤600℃). Figure 3 shows the schematic cross-sections of the major fabrication steps of the UTC-TFT technology with complementary devices. Silicon wafers with 800nm thermally grown oxide were used as the starting substrates. Firstly, the thermal oxide is patterned by dry etching to form the grooves with a depth about 300nm as the thick drain/source region, as shown in Fig. 3(a). Then, a 200nm a-Si film was deposited at 550℃ by LPCVD, then a second 200nm a-Si film was deposited after the phosphorus (Dose= 5×10^{15} cm^{-2}) and boron (Dose= 1×10^{16} cm^{-2}) implantation, respectively. Subsequently, the wafers were chemo-mechanically polished (CMP) down to the oxide polish stop layer as Fig. 3(b). After that, a 30nm a-Si film for the channel region was deposited at 550℃ by LPCVD, and patterned by dry etching. The deposited a-Si films were then recrystallized for 20 hours in nitrogen ambient at 600℃. Along

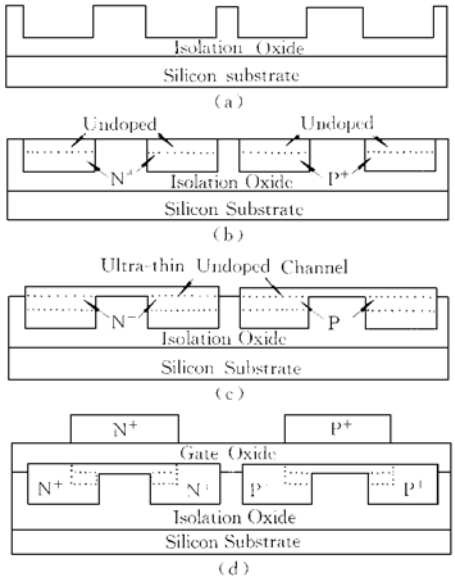

FIG. 3 Schematic Cross-Section and Major Fabrication Steps of UTC-TFT Technology

with the recrystallization, the second deposited silicon film was lightly doped due to the diffusion of phosphorus and boron from the bottom layer, as is shown in Fig. 3(c). After a 100nm APCVD gate oxide deposition, a 200nm gate poly-Si was deposited and patterned. The phosphorus (Dose= $5\times10^{15}cm^{-2}$) and boron (Dose= $1\times10^{16}cm^{-2}$) implantation were then done again, respectively, to heavily dope the gate and drain/source contact regions. A 0.4μm thick LTO then succeeded to deposite, and the contact holes to gate, source and drain were defined after the LTO densification at 600℃ for 10 hours in oxygen ambient. The dopants were also activated during the densification of the LTO. The wafers were sintered at 400℃ after the metallization and patterning. Finally, the devices were hydrogenated in H_2 RF plasma for 2 hours. It is seen that the fabrication process for UTC-TFT is in agreement with the conventional commericial TFT one, except that an extra CMP step is necessary. CMP technology has been commonly employed in VLSI for multilevel metallization, shallow trench insulation and so on. Here it was only for the formation of the thick drain/source regions. It was not a critical step of determining the thickness of the channel as that in the ECTFT technology[10] in which ultra-thin film was impossible, and the ultra-thin channel with uniform thickness can be obtained here simply by LPCVD.

4 Results and Discussion

Figure 4 shows the experimental I-V characteristics of the complementary UTC-TFTs and conventional TFTs with uniform thickness film fabricated along with the UTC-TFTs. The channel region thickness (t_{ch}) of the UTC-TFTs is 30nm, and those of the conventional TFTs are 30nm and 120nm. It can be seen that the conventional TFT with thick channel (120nm) does not exhibit a severe kink effect. The conventional TFT with ultra-thin channel (30nm) shows the good current saturation at low biases, but a severe kink at higher biases. However, for the novel UTC-TFTs, kink effect is suppressed significantly even at high biases (e.g. at V_{gs}= 20V, V_{ds}= 30V for n-channel, and V_{gs}= 20V, V_{ds}= 20V for p-channel), and excellent saturation characteristics are obtained. It is suggested that the moderate kink in the thick film device should be mainly due to the relatively low electrical field in the channel near the drain, since the electric field decreases with the decrease of the channel thickness for the conventional devices because of the two-dimension effect[9]. For the conventional ultra-thin TFT, the good current saturation at the low drain biases is the result of the fully-depletion at the channel[16], while the severe kink at high drain biases results from the exaggerated avalanche multiplication by the high drain field and the large amount of grain-boundary traps. The excellent saturation characteristics in the UTC-TFT are attributed to the combination of the effective reduction in the drain electric field (shown in Fig. 4) with the fully-depletion in the ultra-thin channel.

Figure 5 shows the experimental gate transfer characteristics of various TFTs. It can be seen the UTC-TFTs exhibit the best device performances. In comparison with the thick channel TFT (t_{ch}= 120nm), the UTC-TFTs have about 2.5 times (for n-channel, at V_{gs}=

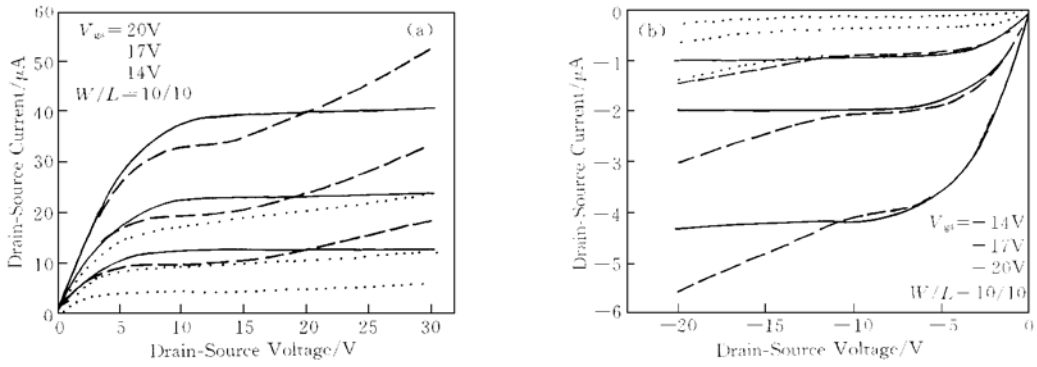

FIG. 4 Experimental I–V Characteristics of Complementary UTC-TFT and Conventional TFT. (a) n-Channel, (b) p-Channel. The solid, dashed and dotted lines are for UTC-TFT (t_{ch}= 30nm), converntional TFT(t_{ch}= 30nm) and conventional TFT (t_{ch}= 120nm), respectively.

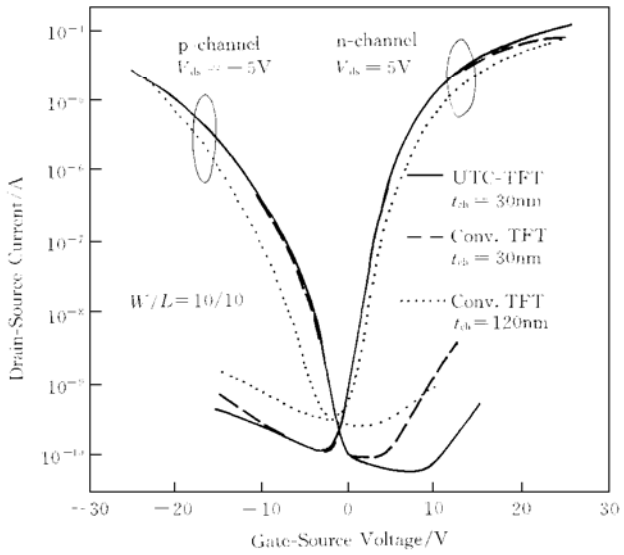

FIG. 5 Experimental Gate Transfer Characteristics of Complementary UTC-TFTs and Conventional TFTs.

10V and V_{ds}= 5V) and 4.5 times (for p-channel at V_{gs}= − 10V and V_{ds}= − 5V) increase in on-current, 3.5 times (for n-channel) and 5 times (for p-channel) reduction in the minimum off-current, and 1.6 times increase in carrier mobility. Among the two ultra-thin film devices, the UTC-TFT also has lower off-current (38%) at high reverse gate biases (V_{gs}= − 15V) since the lower drain field, and the higher one (18%) at high forward gate biases (V_{gs}= 20V) the better source/drain contacts. The device characteristics for various TFTs are summarized in Table 1.

Table 1　Major Device Characteristics

Devices	V_{th}/V (100nA×W/L)	Sth. voltage swing /(V/Dec.)	μ_{FE} /($cm^2 \cdot V^{-1} \cdot s^{-1}$)	I_{off} /(pA·μm^{-1})	I_{on}/I_{off} Ration×10^6
n-UTC-TFT	2.5	1.25	36	10.1	1.2
p-UTC-TFT	-8	1.71	11	5.01	0.55
n-conv. TFT(30nm)	2.5	1.25	36	10.1	0.78
p-conv. TFT(30nm)	-8	1.71	11	8.95	0.31
n-conv. TFT(120nm)	3.2	1.28	23	32.8	0.26
p-conv. TFT(120nm)	-10.5	2.22	7	22.3	0.12

It is necessary to point out that short-channel devices are more suitable for the high-speed digital circuit applications since they provide with both large driving current and small device areas. However, those devices fabricated with the conventional technology suffer from a low drain breakdown voltage that can not satisfy the digital circuits driving requirement. For the poly-Si TFT-LCD, a 15V power supply is required at least. Figure 6 shows the experimental breakdown voltage as a function of gate length for the novel UTC-

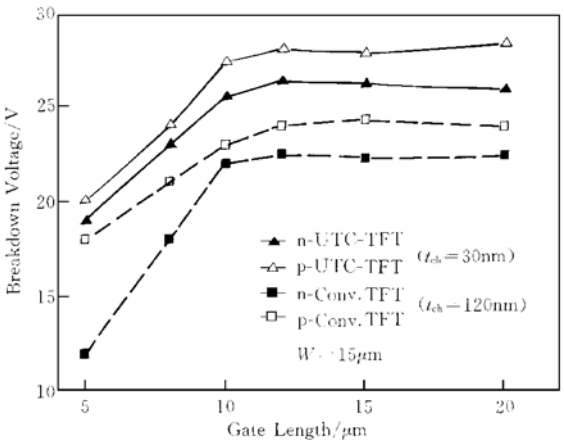

FIG. 6　Experimental Breakdown Voltage as a Function of Gate Length for UTC-TFTs and Conventional TFTs.

TFT (30nm) and the conventional TFT. The breakdown voltage is defined as the V_{ds} at I_{ds} = 2nA and V_{gs}= 0V. The breakdown voltage of the conventional n-channel TFT decreases from 22V to 12V when the gate length reduces from 10μm to 5μm. However, for the UTC-TFT with 10μm and 5μm gate lengths, breakdown voltages of 26V and 19V are obtained, respectively. The high breakdown voltage is also attributed to the low peak electrical field at the drain. The improved breakdown characteristics imply that the novel UTC-TFT devices can be scaled down for the high performance digital circuit applications.

5 Conclusion

In this paper, a novel low temperature ultra-thin poly-Si device technology is proposed and experimentally demonstrated. The superior device performances of the novel UTC-TFT are also experimentally verified. Experimental results indicate that the newly proposed technology provides LTPS TFT devices with both excellent current saturation characteristics and high drain breakdown voltage in short channel devices. Moreover, the on- and off-current characteristics of LTPS device are also improved significantly. All of these show the proposed technology can be used to implement the high performance digital and analog circuits for fully-integrated AM-LCD system on glass.

References

[1] K. Werner, IEEE Spectrum, 1997, **34**(5): 45—49.

[2] 葛长军, 靳在渊, 成建波, 半导体学报, 1999, **20**(3): 254—259[GE Changjun, JIN Zaiyuan, CHENG Jianbo, Chinese Journal of Semiconductors, 1999, **20**(3): 254—259(in Chinese)].

[3] 熊绍珍, 赵 颖, 王宗畔, 等, 半导体学报, 1997, **18**(10): 771—775[XIONG Shaozhen, ZHAO Ying, WANG Zongpan *et al*., Chinese Journal of Semiconductors, 1997, **18**(10): 771—775(in Chinese)].

[4] Y. Matsueda, S. Inoue, S. Takenaka, S. Ozawa, S. Nakazawa and N. Ohshima, Dig. SID Int. Symp., 1996, 89—92.

[5] F. Kato, M. Yotsuyanagi, M. Ishida, K. Kitamura and S. Saito, Dig. SID Int. Symp., 1996, 247—250.

[6] A. G. Lewis, D. D. Lee and R. H. Bruce, IEEE J. Solid-State Circuits, 1992, **27**(12): 1833—1841.

[7] H. G. Yang, S. Fluxman, C. Reita and P. Migliorato, IEEE J. Solid State Circuits, 1994, **29**(6): 727—732.

[8] M. Miyasaka, T. Komatsu, W. Itoh, A. Yamaguchi and H. Ohashima, Extended Abstract of SSDM, 1995, 647—650.

[9] M. Yoshimi, M. Takahashi, T. Wada, K. Kato, S. Kambayashi, M. Kemmochi and K. Natori, IEEE Trans. Electron Devices, 1990, **37**(9): 2015—2020.

[10] A. Kumar K. P. and J. K. O. Sin, IEDM Tech. Digest, 1997, 515—518.

[11] M. Takabatake, J. Ohwada, Y. Ono, K. Ono, A. Mimura and N. Konishi, IEEE Trans. Electron Devices, 1992, **38**(6): 1303—1309.

[12] J. P. Colinge, Electron. Lett., 1986, **22**: 187—188.

[13] M. Hack and A. G. Lewis, IEEE Electron Device Lett., 1991, **12**(5): 203—205.

[14] K. Tanaka, H. Arai and S. Kohda, IEEE Electron Device Lett., 1988, **9**(1): 23—25.

[15] "MEDICI User's Manual, Version 1", Technology Modeling Associates, Inc., 1992.

[16] J. P. Colinge, IEEE Electron Device Lett., 1988, **9**(2): 97—99.