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Growth of Thin Silicon on Sapphire (SOS) Film Materials and Device Applications

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Abstract: The increasing emphasis on the sub-micron CMOS/SOS devices has placed a demand for high quality thin silicon on sapphire (SOS) films with thickness of the order 100- 200nm. It is demonstrated that the crystalline quality of as-grown thin SOS films by chemically vapor deposition method can be greatly improved by solid phase epitaxy (SPE) process: implantation of self-silicon ions and subsequent thermal annealing. Subsequent regrowth of this amorphous layer leads to a great improvement in silicon layer crystallinity and channel carrier mobility, respectively by double crystal X-ray diffraction and electrical measurements. Thin SPE SOS films would have application to the high-performance CMOS circuitry.

Key words: silicon; epitaxial growth; solid phase epitaxy
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薄层 SOS 薄膜材料外延生长及其器件应用

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摘要: 亚微米 CMOS/SOS 器件发展对高质量的 100- 200 纳米厚度的薄层 SOS 薄膜提出了更高的要求. 实验证实: 采用 CVD 方法生长的原生 SOS 薄膜的晶体质量可以通过固相外延工艺得到明显改进. 该工艺包括: 硅离子自注入和热退火. X 射线双晶衍射和器件电学测量表明: 多晶化的 SOS 薄膜固相外延生长导致硅外延层晶体质量改进和载流子迁移率提高. 固相外延改进的薄层 SOS 薄膜材料能够应用于先进的 CMOS 电路.

关键词: 硅; 外延生长; 固相外延

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1 Introduction

Silicon on insulator (SOI) is the technology drawing an increasing attention to the next generation integrated circuits, which requiring significantly-reduced power dissipation and gate delay along with the increased packing density and isolation. Furthermore, since the lateral scaling is continuing, vertical dimensions must be reduced. Both n^+ and p^+ source/drain regions of 100nm deep or less should facilitate the design and fabrication of the sub-500 nm gate length MOSFETs with long channel behavior. The device and processing advantages which result from the high quality silicon films on the insulator are the motivation for development of the thin silicon on sapphire (SOS) technology.

UP to date, SOS is one of the most mature SOI technologies[1] with following advantageous characteristics: large area single crystal film, full dielectric isolation with virtual zero substrate capacitance, a track record for the application of VLSI and commercially availability of well characterized materials. However, it has been known that the as-grown chemically vapor deposition (CVD) SOS films contain a large number of crystalline defects such as dislocations, stacking faults and microtwins[2]. These planar defects are formed at the early stage of the epitaxial silicon film growth due to the lattice mismatch between the sapphire substrate and the silicon epilayer, and/or the reaction between the substrate and the deposition constituents[3]. Normally the defect density increases with the SOS film thickness decreasing or near the silicon/sapphire interface. These defects lead to the decrease of carrier mobility and the large leakage current in CMOS/SOS devices, and therefore the electrical performance of SOS devices have deteriorated. The improvement of SOS/CMOS devices performance is rather limited though the modified device design rules are utilized in the fabrication of CMOS/SOS. Better device results[4,5] were recently reported on the CMOS circuits fabricated in the improved 0.5μm thick SOS materials by solid phase epitaxy (SPE). Nevertheless, reducing SOS film thickness to 200nm below requires more significant material improvement near the silicon/sapphire interface; also, applying thin SOS films to CMOS devices requires novel process development.

The crystal quality of SOS film material and the electrical characteristics of SOS/CMOS device can be improved markedly by optimized epitaxial growth process and furthermore the incorporation of SPE processes[6—8]. In our research, the relatively high quality as-grown thin SOS films with thickness of 200nm below were fabricated by modified vapor phase epitaxial growth process. Then, solid phase epitaxial regrowth process: implantation of self-silicon ions and subsequent thermal annealing, were incorporated into further improve the crystal quality of thin SOS films. The enhanced-mode CMOS/SOS devices were fabricated on the improved thin SOS films. The film quality was characterized

by Double-Crystal X-Ray Diffraction (XRD) and electrical measurement of CMOS devices. It is demonstrated that the device quality thin SOS epitaxial films have been fabricated by SPE process and have application to the advanced CMOS devices.

2 Experimental Procedures

2.1 Thin SOS Material Growth and Improvement

The thin SOS material improvement procedure consists of two steps: an initial vapor phase epitaxial growth of thin SOS films and a solid-phase regrowth of that after the implantation with silicon. The SOS films with thickness of 200nm below were grown on a horizontal vapor phase epitaxial reactor via prolysis of silane-hydrogen mixtures in the hydrogen ambient at temperature of 980℃. The substrate was $(1\bar{1}02)$-oriented polished sapphire wafer of 1.5 inch in diameter. The silicon epi-layers were intrinsic without any doping. The relatively high quality as-grown SOS films were obtained by modified dual-growth-rate epitaxial process: firstly, silicon epilayers were deposited at a higher growth rate in the initial nuclei/growth stage in order to realize a more uniform coverage of the sapphire substrate, then to obtain desired SOS film thickness at a lower growth rate.

In the second step, the as-grown 200nm SOS films are first implanted with $^{29}Si^{+}$ ions to amorphize most of the Si layers and then regrown epitaxially in the solid phase. In order to compare the SPE SOS films with the non-SPE SOS films, half of an as-grown SOS wafer was Si^{+} ion-implanted and the other half was masked without implanted (as the controlled sample). Then the whole SOS wafer was subsequently annealed for SPE regrowth and for CMOS device fabrication. The Si^{+} ions were implanted at room temperature with energy of 70 keV. A total dose of 2×10^{15} cm^{-2} was used to make the thin silicon layer sufficiently amorphous and avoid the excess damage of the silicon/sapphire interface during Si^{+} ion implantation. The implanted SOS wafer would be annealed for 30min at 1000℃ in nitrogen ambient. In the annealing process, the solid-phase epitaxial regrowth of the amorphous Si layer might occur.

The crystalline quality of the SOS films was examined by double-crystal X-ray diffraction. The double-crystal spectrometer (Model: SLX-1AL, J. Rigaku) was used to measure the diffraction spectra and the linewidth at half its maximum intensity referred to as "FWHM". In such measurements of SOS layers, the (400) Si reflection is commonly used from the plans parallel to the wafer surface. The broadening of the diffraction peak implies the misorientations between the adjacent crystalline regions. This misoritation is associated with the dislocations in the silicon layers.

2.2 CMOS/SOS Device Fabrication

In order to determine whether the crystalline improvements on thin SPE/SOS films had been transferred into MOS device improvements, the SOS wafers were used for the

Table 1 Fabrication Process Characteristics for n- and p-MOS Devices

parameters		n-channel	p-channel
t_s		200nm	200nm
t_{ox}		50nm	50nm
Channel Implants	A	75keV, 2×10^{11}cm^{-2}	150keV, 2×10^{11}cm^{-2}
	B	75keV, 6×10^{11}cm^{-2}	150keV, 4×10^{11}cm^{-2}
S/D implants		P: 100keV, 5×10^{11}cm^{-2}	B: 60keV, 5×10^{11}cm^{-2}
L		2μm	2μm
W		26μm	26μm

fabrication of dual-enhanced mode CMOSFETs. The fabrication consisted of silicon island definition, channel implants, gate oxidation, boron-doped polysilicon deposition and definition, N^+ and P^+ source/drain implants, contact opening, and metalization in sequence. Boron was implanted at 75keV, 2×10^{11} cm^{-2} (type A) and 6×10^{11} cm^{-2} (type B) respectively, and the phosphorous at 150keV, 2×10^{11} cm^{-2} (type A) and 4×10^{11} cm^{-2} (type B) respectively, as were used to dope the n- and p-channel regions. The thickness of silicon film and of gate oxide layer were 200nm and 50nm respectively. Boron-implants at 60keV, 5×10^{15} cm^{-2} and phosphorous-implants at 100keV, 5×10^{15} cm^{-2} were used to dope the source and drain regions for the p- and n-channel MOSFETs respectively. The length and width of n- or p-channel were 2μm and 26μm, respectively. The fabrication process characteristics for MOS/SOS device are summarized in Table 1.

3 Results and Discussions

3.1 X-Ray Diffraction Analysis of Thin SOS Films

Figure 1 shows the double-crystal X-ray diffraction spectra of thin as-grown SOS and SPE SOS films as well as the controlled SOS films. For comparison, Fig. 1 (d) also shows

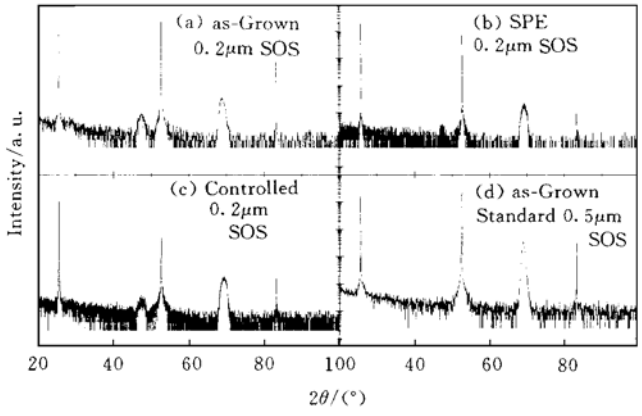

FIG. 1 Double-Crystal X-Ray Diffraction Spectra of SOS Films

the spectrum of a standard 0.5μm-thick as-grown SOS film. In the 2θ ranging between 20 – 100, there is only one diffraction peak for Si(400) at 2θ= 68.9 besides the three peaks at

25.6, 52.65, 83.2 respectively for sapphire $(\bar{1}102)$, $(\bar{2}204)$ and $(\bar{3}306)$ planes. This result indicates that the epitaxial crystalline relationship between silicon layer and sapphire substrate is (100) Si // $(\bar{1}102)$ Al_2O_3 for the standard thick SOS films, and the silicon epilayer on sapphire substrate is a single crystalline phase. The (400) Si peak is very sharp and its FWHM is only 0.365 degree. This also confirms that the standard thick SOS films have a higher crystalline perfection. In contrast, there appears two diffraction peaks: one intensive peak Si(400) at $2\theta = 68.9$ and the other small one Si(220) at $2\theta = 47.35$ in the XRD spectrum of thin as-grown SOS films (as shown in Fig. 1(a)). Part of the broadening was observed in the Si (400) diffraction line and its intensity decreased to some degree in comparison with the standard-thick SOS films. It is demonstrated that for 0.2μm SOS films, apart from the dominant growth along < 100> orientation, there exists competitive silicon epitaxial growth along < 110> orientation perpendicular to the sapphire $(\bar{1}102)$ surface at the initial growth stage of silicon epilayers at the interface of silicon/sapphire. As the epitaxial growth keeps continued, the thickness of SOS films would increase. As a result, the epitaxial growth along < 110> orientation is restrained and disappears finally, and therefore a single crystalline phase (100) Si will formed on the sapphire substrate for the standard 0.5μm SOS films. This result shows that the crystalline perfection of 0.2μm SOS films is not better than that of 0.5μm ones due to the loss of favorable (100) oriented Si planes to (110) oriented planes.

In order to improve the crystalline perfection of thin SOS films, Si^+ ion self-implantation and SPE regrowth by high temperature annealing were incorporated. As shown in Fig. 1(b), the diffraction line intensity of (110) Si planes was observed to decrease greatly and almost disappear after the SPE regrowth. In contrast, the XRD spectrum of controlled 0.2μm SOS films was shown in Fig. 1(c). It is observed that the decrease in the diffraction line intensity of (110) oriented planes is inconspicuous. These results show that a majority part of the (110) oriented Si planes in as-grown SOS films are transformed into (100) oriented planes after SPE process, and therefore a single crystalline phase (100) oriented Si epilayer was formed. It is obvious that the crystalline perfection of 0.2μm SOS films has been improved by SPE.

3.2 CMOS/SOS Device Performances

3.2.1 Channel Leakage Current Characteristic of the MOSFETs

The electrical performances of the CMOS devices fabricated in both 0.2μm SPE SOS films and controlled SOS films have been measured. We summarized the electrical parameters of NMOSFETs and PMOSFETs in Table 2. I_{DSS}, V_T and BV_{DSS} shown in Table 2 are the channel leakage current, threshold voltage and source-drain breakdown voltage respectively. The results show that the channel leakage current for either NMOS or PMOS device decreases markedly after the improvement of 0.2μm SOS film materials by SPE process, though there is no distinct change for the other parameters of devices.

Table 2 Electrical Characteristics of CMOS/SOS Devices

Mode	Type		V_T/V	$I_{DSS}/10^{-12}$A · μm^{-1} (V_{DS}= 5V)	BV_{DSS}/V
NMOS	A	SPE SOS	1.6	**2.3**	18
		Controlled	1.8	**6.9**	18
	B	SPE SOS	1.8	**2.7**	18
		Controlled	2.5	**7.7**	18
PMOS	A	SPE SOS	− 1.2	**1.9**	25
		Controlled	− 1.8	**5.7**	24
	B	SPE SOS	− 2.0	**2.3**	28
		Controlled	− 2.4	**5.7**	25

3.2.2 Channel Carrier Mobility Characteristic

Based on the electrical parameters of both the CMOS devices in 0.2μm SPE and the controlled SOS films, the carrier mobility of n-type and p-type SOS films was determined by the following formula:

$$\mu = (I_{DS}t_{OX}L)/(W\epsilon_{OX}\epsilon_0)[(V_{GS} - V_T)V_{DS} - (V_{DS}^2/2)]$$

Where I_{DS} is the source-drain current, t_{OX} is the gate oxide thickness, V_{GS} is the gate voltage, V_T is the threshold voltage, W and L are the channel width and length, ϵ_{OX} and ϵ_0 are the relative dielectric constant and vacuum dielectric constant, respectively.

Figure 2(a) and Figure 2(b) show the electron and hole carrier mobility improvement of 0.2μm SOS films after SPE process respectively. In comparison, the hole mobility increases in a small magnitude, whereas the electron mobility increases more significantly. It is evident that a higher carrier mobility of CMOS devices is achieved by the crystal quality improvement of 0.2μm SOS films materials through the optimized ion implantation and SPE regrowth.

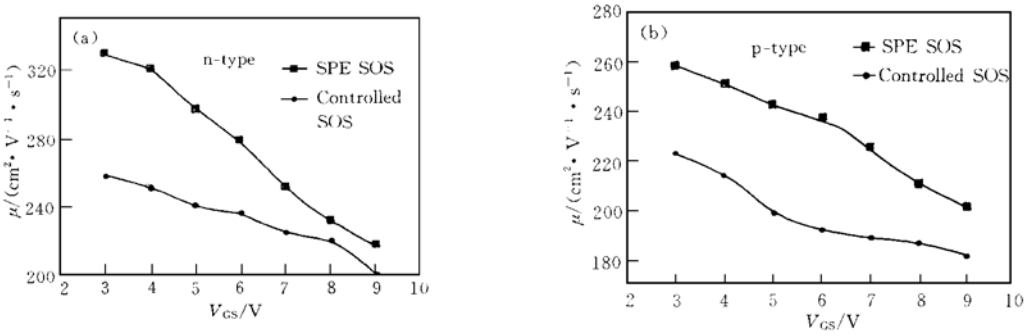

FIG. 2 Electron (a) and Hole (b) Carrier Mobility of SPE and Controlled SOS Films Versus Gate Voltage

3.2.3 Source-Drain Output Characteristic

Figure 3(a) and Figure 3(b) are respectively the source-drain output characteristic of NMOS devices fabricated on 0.2μm controlled and the SPE SOS films. From Fig. 3 it is clearly observed that the source-drain output currents of NMOSFETs on SPE SOS films increase above 5mA. It is demonstrated that due to the crystalline improvement of SOS films, the carrier mobility will increase and therefore lead to the improved output currents.

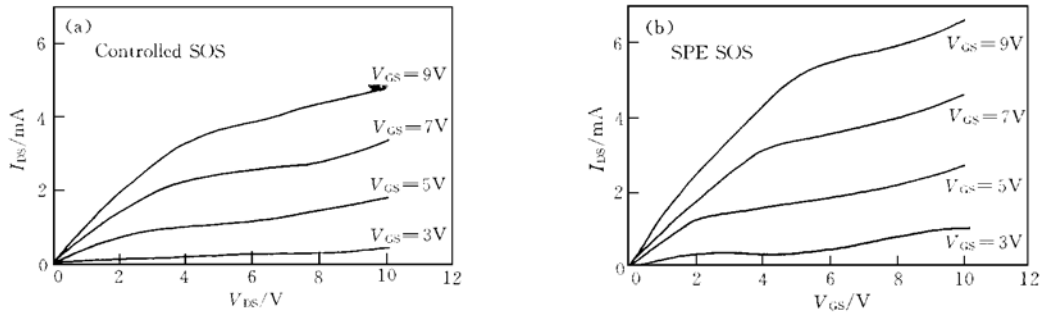

FIG. 3　Source-Drain Output Characteristic of NMOS Devices Fabricated on 0.2μm Controlled (a) and SPE (b) SOS Films

3.2.4 Sub-Threshold Voltage Characteristic

The sub-threshold voltage characteristic of MOSFETs was measured and shown in Fig. 4, which are fabricated in 0.2μm SPE the controlled SOS films. We compared them and it is noticed that the source-drain current of MOS devices fabricated in 0.2μm SPE SOS is smaller than that of identical devices in the controlled SOS when V_{gs} is below the threshold voltage. Also, the slop of I_{GS} versus V_{GS} curve is higher than that of devices in controlled SOS. It shows that there exists a distinct improvement in the sub-threshold voltage characteristic of CMOS devices after SOS film materials improvement.

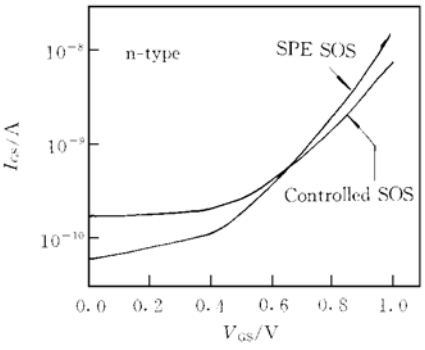

FIG. 4　Sub-Threshold Voltage Characteristic of NMOS Devices Fabricated in Controlled and SPE SOS Films

4 Conclusion

The high quality 0.2μm SOS films were obtained by ion-implantation and SPE regrowth processes. The SPE process can effectively eliminate the crystal defects in as-grown SOS films and improve the crystalline quality of SOS materials as well as the electrical performance of CMOS/SOS devices. The electrical measurements of MOSFETs on SPE SOS films show that the carrier mobility increases

significantly and the leakage current, source-drain output and threshold characteristics are improved to a certain extent. We conclude that the improved thin SOS films of the order of 0.2μm in thickness by SPE is suitable for the application in some high performance CMOS circuits.

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