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A Monolithically Integrated 12V/5V Switch-Capacitor DC-DC Converter*

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Abstract: A monolithically integrated 12V/5V switch capacitor DC-DC converter with structure-simplified main circuit and control circuit is presented. Its topological circuit and basic operating principle are discussed in detail. It is shown that elevated operating frequency, increased capacitance and reduced turn-on voltage of the diodes can make the converter's output characteristics improved. Reducing resistance of the equivalent resistors and other parasitic parameters can make the operation frequency higher. As a feasible efficient method to fabricate monolithically integrated converter with high frequency and high output power, several basic circuits are parallelly combined where the serial-parallel capacitance is optimized for the maximum output power. The device selection and its fabrication method are presented. A feasible integration process and its corresponding layout are designed. All active devices including switching transistors and diodes are integrated together with all passive cells including capacitors and resistor on a single chip based on BiMOS process, as has been verified to be correct and practical by simulation and chip test.

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1 Introduction

Motivated by the battery-operated applications that demand compact, lightweight and efficient DC-DC converters, many kinds of converter circuits have been published. Among them, resonant converters and the soft-switching converters have greatly reduced switching losses in comparison to the conventional switching, because of the power switches turning on at zero voltage or turning off with zero current. However, it is very difficult for them to

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integrate because of their bulky inductive elements. Moreover, magnetic cells not only complicates the design, but also introduces second-order effects in converter circuits. The switch-capacitor (SC) DC-DC converters have some advantages such as the simplified structures, easy to be controlled, etc. Furthermore, the most attractive advantage is that there is no inductive cell in the converter circuits, which makes DC-DC converters be available for the monolithic integration. Also, the SC DC-DC converter can operate in a higher frequency without resonant circuits because of the elimination of the turn-off losses caused by inductors. Some kinds of integrated SC DC-DC converters such as MAX662A, MAX860 and TC7660, etc, have been developed, which are usually called as charge-pump. But they all have a common characteristic that only control circuit and main power switches are integrated on the chip while capacitors have to be connected outside the chip, which limits the utilization of the converters. Monolithically integrated SC DC-DC converters with their capacitors on same chip are needed in some pocket power supply systems, which demand a high interference-resistance capability. There exist some difficulties in the monolithic integration design. For example, in order to obtain higher output power, a compromise has to be made between operation frequency, output power and conversion efficiency, meanwhile a suitable process must be estabilished to fabricate the big capacitors with high quality. Perhaps for such a reason, optimizing for the design of monolithic integrated SC DC-DC converters has not been reported yet.

In this paper, we present a monolithically integrated 12V/5V SC DC-DC converter. Its topological circuit and basic operating principle are discussed theoretically. The relationship between the capacitance of its constituent capacitors, the switching frequency and the output power is analyzed to make a good compromise. It is shown that elevated operating frequency, increased capacitance and reduced turn-on voltage of the diodes can make the converter's output characteristics improved. As an efficient method proposed to fabricate a monolithically integrated converter with high frequency and high output power, we parallelly combine several basic circuits. The device selection and its fabrication method are presented. A feasible integration process, including fabrication method of high-qualified capacitors and the corresponding layout are designed. All active devices, including switching transistors and diodes, are integrated together with all passive cells on a single chip, as minimizes the size of the converter.

2 Basic Principle

The topological circuit of the integrated 12V/5V SC DC-DC converter is schematically shown in Fig. 1. It consists of a control circuit and a conversion unit, which has been presented and discussed in detail elsewhere[2]. The circuit operates in two states when the capacitors being charged and discharged, respectively. In order to fabricate the converter operating in high frequency and high output in the way of monolithic integration, we have proposed of feasible method to combine several basic conversion circuit-units in parallel.

Solving the differential equations of the circuit, we can write the output power of one unit of the 12V/5V SC DC-DC converter as

$$P_{out} = 2f C_1 V_L \left(\frac{V_S}{2} - \frac{3V_d}{2} - V_L \right) \frac{1 - e^{-\frac{1}{2fRC}}}{1 + e^{-\frac{1}{2fRC}}} \tag{1}$$

Where f is the operating frequency of the converter, C_1 is the capacitance of the serial-parallel (SP) capacitors $C11$ and $C12$, have the same value, V_d is the forward bias voltage of the diodes, R and C are equivalent resistance and capacitance of the circuit, which can be usually considered approximately to be same in its two different states, respectively. $2fRC$ in the equation (1) is much smaller than 1 because the capacitance, which can be realized in a general monolithic integration process, is only pF order of magnitude in usual. Description of the output power, therefore, can be simplified as

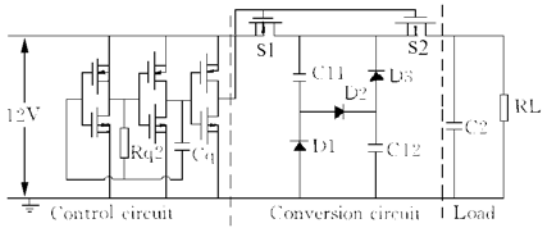

FIG. 1　Basic Configuration of Integrated 12V/5V SC DC-DC Converter

$$P_{out} = 2f C_1 V_L \left(\frac{V_S}{2} - 3\frac{V_d}{2} - V_L \right) \tag{2}$$

The equation indicates that a higher output can be obtained by using an elevated operating frequency and bigger capacitance as well as lower on-state voltage of the diodes.

3　Design for Integration

The major parameter of the 12V/5V SC DC-DC converter are f, C_1 and V_d. A compromise must be made for f between output power and conversion efficiency because raising frequency not only gets output power increased but also heightens the energy losses of the switches and reduces the converter's efficiency. We don't think the operating frequency would be higher than 10MHz[2]. The SP capacitance C_1 is chosen to be 50pF in one unit circuit because bigger capacitors are not suitable to be fabricated in monolithic integration technology. For the application of the converter at a low voltage with low current, MOSFET is better to be chosen as the switches. To simplify the gate-driven circuit, a P-MOS is chosen to be S_1 and S_2 is designed as a N-MOS. The diodes must satisfy the demands for low on-state voltage and high switch speed. Schottky Barrier Diode (SBD) is selected to meet the needs.

All devices in the circuit can be compatibly realized in a standard integration process. Fabrication of the active devices is relatively easy, while making the capacitors becomes a key problem. In order to make the capacitors as large as possible on a limited chip area, dual-layer structures are used as shown in Fig. 2. To the whole capacitor, the poly 1 acts as one electrode, meanwhile the diffusion layer and poly 2 which are connected in series act as another electrode of the capacitor. Specific capacitance of the capacitor is calculated to be

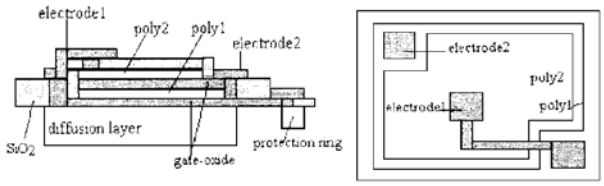

FIG. 2 Structure of Capacitor

6.9×10^{-4} pF/μm^2 when the thickness of dielectric is 100nm.

Aluminum is deposited on the surface of N^- substrate to form a metal-semiconductor rectifying contact that constitutes SBDs. The three diodes in one unit circuit are isolated eash other by reverse biased p-n junctions. Therefore, the devices are made on the different N-type epi-islands.

The ion implantation technology was utilized to fabricate the resistor in the driving circuit. In order to get more testing results, its resistance was designed to be different from chips to chips to obtain different operation frequencies. For the purpose, 4 kinds of dopants were used to make different resistors so that no extra mask was required. Specific resistance designed for different resistors are 0.5kΩ/□, 0.7kΩ/□, 1.2kΩ/□ and 2.4kΩ/□, respectively. Their corresponding oscillation frequencies are 2.4MHz, 1.7MHz, 1MHz and 500kHz, respectively.

According to the calculation for one unit, the maximum output current is 200μA when the operation frequency is 2MHz and the capacitance 50pF. In our fabrication, we combine 11 units in parallel with a common driving circuit. The maximum output current of the converter should be 2mA.

4 Integration Process

A P-well Si-gate CMOS technology was employed to fabricate some test chips of the monolithically integrated 12V/5V SC DC-DC converter. P-type silicon wafers were chosen as original materials. The lower isolation region and the burial layer were formed in a diffusion process prior growing the N-type epitaxial layer. The devices that need to be isolated were fabricated in the N-type islands isolated by reverse biased p-n junctions. The manufacturing procedure is shown in Fig. 3. In comparison with a basic P-well CMOS process, some extra steps such as formation of epitaxial layer, the antimony burial layer, the boron burial layer and the second polysilicon was introduced. The process needs 15 photolithographic masks, and the seventh one, was used to remove SiO_2 previously grown so as to let a new SiO_2 layer with more compact texture to be grown for the MOS capacitors. Owing to the SiO_2 layer accumulated on the contacts in the two steps for gate-oxide formation might be too thick to be etched, the ninth mask was designed for etching the contact windows and the active regions of MOSFET as well. The P^+ diffusion layer that acts one electrode of the capacitor is surrounded by N^+ protecting ring, to which the highest voltage is applied for isolation of the capacitor from other devices. The resistor formed by N^+ ion implantation was made in the P-well surrounded by a P^+ protecting ring. The second polysilicon is also used as the gate of the MOS transistor. The N^+ burial layers underneath

the MOS transistors were designed to prevent from the latch-up affection. SBD was made on the epitaxial layer and isolated by the reverse biased p-n junctions. Under metal-semiconductor contact there also exists a N^+ burial layer to eliminate the parasitic series resistors of SBD. Cross-section of the devices in the integrated 12V/5V SC DC-DC converter is shown in Fig. 4 to demonstrate their structure.

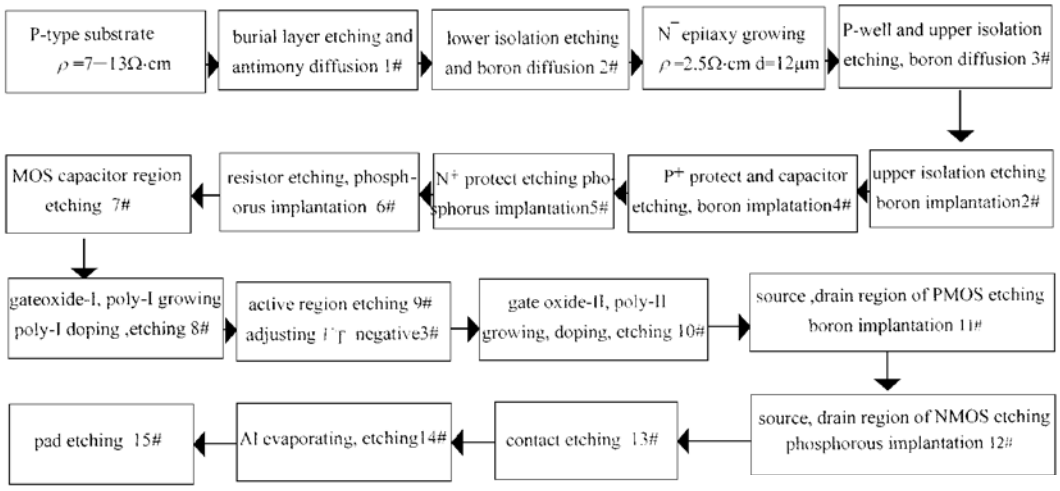

FIG. 3　Integration Technology Process

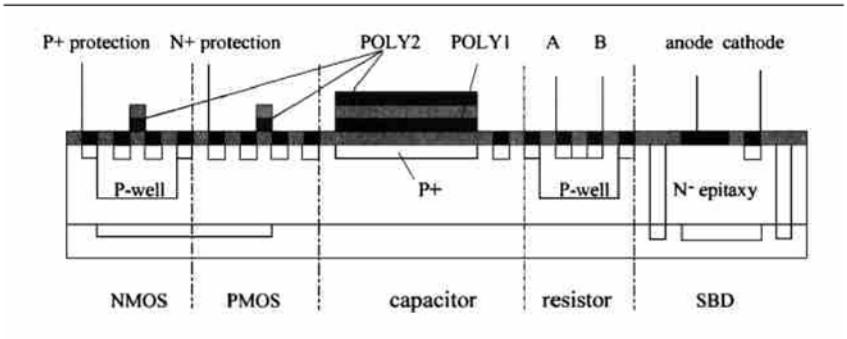

FIG. 4　Device Structure Profile

5　Layout Design and Verification

6μm P-well Si-gate CMOS technology was used to fabricate the monolithically integrated converter, which means the channel length L of MOSFETs in the converter is 6μm. The threshold voltage was designed to be 1V for the NMOS and − 1.4V for the PMOS, respectively. The theoretical cut-off frequency decided by the channel length was calculated to be about 1400MHz according to

$$f_T = \frac{2\mu}{4\pi L^2}(V_{GS} - V_T) \tag{3}$$

which is much higher than what designed for the converter.

Different methods were used to determine the channel width W of the MOSFETs in main circuit and drive circuit, respectively. The main circuit was defined from switched current while the drive circuit estimated comprehensively from the delay time permitted, the optimal switching response and the maximal pulse current per channel width permitted under a certain process condition. In calculatin, the hole mobility and the electron mobility were chosen as $180cm^2/(V \cdot s)$ and $400cm^2/(V \cdot s)$, respectively, while the thickness of gate-oxide was 100nm according to the integration process.

The main parameters of SBD in this work are saturation current I_s, zero voltage junction capactance C_{J0} and series resistance R_s, which contradictorily depend on the junction area of SBD. Small junction area can result in high speed, little parasitic capacitance and simple IC fabrication process, but large series resistance and high on-state voltage as well. Therefore, a compromise had to be made for the determination of the junction area. In addition, the maximum area of SBD's anode is chosen in layout design because its definition depends on the current that is variable with the operating frequency.

We used software CADENCE to draw the layouts. Considering that a capacitor of 50pF has too big area to prevent from extra leakage, we divided it into two capacitors of 25pF connected in parallel in the layout design. In order to reduce its equivalent series resistors, a lot of contact holes were opened in its electrode plate. The new structure of capacitor introduced a parasitic diode between N^--epilayer and the P^+ diffusion layer that was one of the electrode plate of the capacitor. In order to eliminate the negative affection, N^--epilayer was connected to the anode of power supply through a N^+ protection ring to bias the parasitic diode reversely. Moreover Poly 1 was applied with a lower voltage to eliminate the parasitic depletion capacitance of the MOS capacitor. Considering that there were two high temperature processes in the fabrication, we enlarged the distance between every regions that need to be isolated compared with the usual design to ensure the isolation in good status.

The chip area is about 2.6mm×2.5mm. There are three basic pads, i.e. imput, output and GND, and 4 auxiliary pads that are designed for changing the output power when it is necessary. The other four pads are designed to test the chips more conveniently.

Accuracy of the layout design has been verified in simulation program LVS of CADENCE. All the parasitic devices such as parasitic diodes discussed above have been considered in the simulation. The results coincide with the design requirement very well.

6 Testing Results

Photographs of a nude chip and a packaged chip of the monolithically integrated 12V/5V SC DC-DC converter are shown in Fig. 5. Results of the chips test show that threshold voltage of NMOS and PMOS are 0.9V and −1.4V, respectively, reverse breakdown voltages of MOSFET and SBD are 35V and 45V, respectively, as well. The results coincide

with the design perfectly. However, forward voltage of the SBD is 0.35V at the testing current of 0.1mA, which is higher than a regular value of SBD. It indicates that there might be something to be improved in the fabricating process of metal-semiconductor contact of SBDs. Testing frequencies of the four chips in which four different dopants were used are about 600kHz, 1.1MHz, 1.7MHz and 2.2MHz, respectably. Figure 6 shows one of the testing results. The control pules with frequency of 1.7MHz and the output voltage of 5V are obtained at the input voltage of 12V when a capacitor of 0.1μF and resistor of 5.4kΩ are connected with the output pad and GND in parallel. Then an output power of 4.65mW is obtained. The efficiency value has been tested to be 65%, which is a little lower than the simulation value of 71%. It can be improved by widening the channel of the MOSFET in driving circuit.

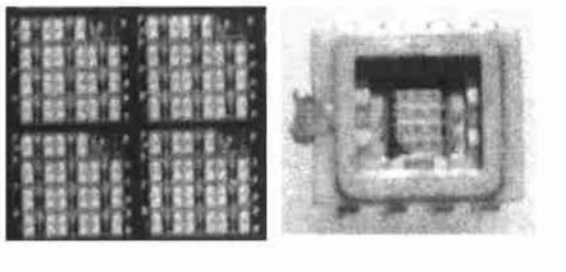

FIG. 5　Photos of Monolithically Integrated Converter

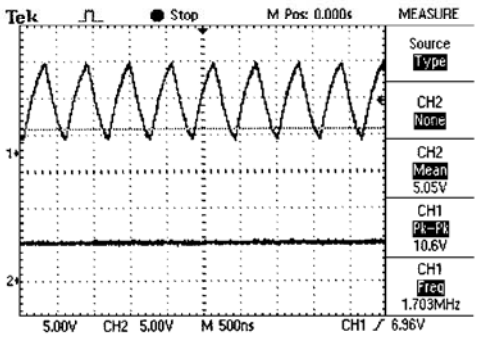

FIG. 6　Testing Results (1) Control Voltage (2) Output Voltage

7　Summary

An efficient method to fabricate monolithically integrated converter with high frequency is proposed in this paper, which is verified by simulation and chip testing. The converter size is reduced through fabricating active and passive devices on a single chip with its interference-resistance capability improved greatly. They are especially suitable for the low-power applications that especially demand compact converters. Even though the output power of monolithically integrated converter is not high, the monolithically integration process has been verified to be feasible and practical. If more units are paralleled, higher power could be obtained.

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