Fabrication of 0.1 Micron MOSFETs and Their Characteristics

YANG Guang(杨 洸) and LIU Li-tian(刘理天)

(*Institute of Microelectronics, Tsinghua University, Beijing* 100084, *China*)

Abstract: Two innovative techniques for manufacturing 0.1 micron MOSFETs are described. One is SiO_2-resist overetching method, in which an additional SiO_2 layer is used to short the gate length; the other is dual-exposure method, according to which two overlapped masks are exposed in a single lithography. Both of them are easy to implement, without any special processing technologies required. The layout used in a real process is introduced. As a result, MOSFETs with minimal channel length of 0.12 micron are obtained. Also, the test results on characteristic are given. Finally, a conclusion is drawn that in 0.1 micron scale, both saturation currents and transconductorance of MOSFETs increase, while substrate currents decrease when channel length diminish.

Key words: SiO_2-resist overetching; dual-exposure method; hot carrier effect; substrate current

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1 Introduction

With the development of IC technology, the device size and power consumption in IC keep decreasing, while the circuit speed is increasing. Recently, in some VLSIs, such as CPU, FPGA and DRAM, the feature lengths have shrunk from 0.35μm to 0.25μm, even 0.18μm, and this trend will last. For such tiny MOS devices used in these ICs, their physical and electrical characteristics are quite different from the micron scale devices[1]. And, much research on the device modeling[2,3] and device structures[4-8] have been done. We developed two novel techniques to fabricate 0.1μm MOSFETs, without utilizing the advanced equipment in this paper. Section 2 describes two novel techniques used for

YANG Guang (杨 洸) was born in 1974. He is now a MS candidate in Institute of Microelectronics, Tsinghua University. He once did research on deep submicron MOSFET fabrication and characteristics research. His current research interest is microprocessor design.

LIU Li-tian(刘理天) was born in 1947. He is a professoir in Institute of Microelectronics, Tsinghua University. He has been focusing at the research on semiconductor devices, integrated circuits and MEMS.

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fabricating 0.1μm MOSFETs; Section 3 gives out both physical and electrical results; in section 4, we analyze the results attained; Finally, a conclusion is drawn.

2 Two New Techniques

To fabricate 0.1μm MOSFETs, the most critical step is to control and gain thin polysilicon gates[9]. According to the present micron or submicron scale technologies, the only way is to combine to current technologies or to apply the current technologies in a non-routine way. In our research, two novel techniques were developed: SiO_2-resist overetching method and dual-exposure method.

2.1 SiO_2-Resist Overetching Method

Gate overetching is a widely used method to get minute gate length. But it is difficult to get good gate intersection shape and hard to control the time for etching polysilicon by using photoresist. Here, we devised an improved method, SiO_2-resist overetching method.

The procedure of SiO_2-resist overetching method is as follows. After polysilicon deposition, an extra layer of SiO_2 was deposit on it by Chemical Vapor Deposition(CVD). The SiO_2 layer was etched or overetched off after normal photolithography. The polysilicon gate was developed by Reactive Ion Etching (RIE) technology using the remaining SiO_2 as resist. After such processes, all problems, which might have happened to polysilicon before, now happen to SiO_2, thus protecting the polysilicon gate.

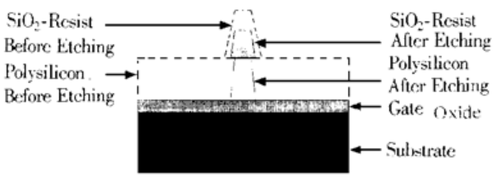

FIG. 1 SiO_2-Resist Over-Etching

SiO_2-resist overetching method does not require high proportion of etching speed of polysilicon to SiO_2. Supposing the proportion is 2, initial polysilicon thickness and SiO_2 thickness are identical, shown with result in Fig. 1.

2.2 Dual-Exposure Method

The dual-exposure method is another innovative technique based on normal technologies. Moreover, it does not require special equipment with high accuracy. Much smaller shape can be gained By using two masks sequentially in one single photolithography. The following is the details of this method.

Give 2μm technology as example (see Fig. 2). In mask Ⅰ, the linewidth is 2μm, while the space between successive two lines is 10μm; in mask Ⅱ, the linewidth is also 2μm, but the space between successive two lines decreases to 9.9μm. So, the width of overlapped shapes varies from 2μm to 0.1μm in a step of 0.1μm. Taking the alignment deviation into consideration, if the mask Ⅱ slides vertically down to the mask Ⅰ by 0.5μm, the width of overlapped shapes will become 1.5, 1.6…, 2.0, 1.9, 1.8…, 0.6μm, i.e. the minimum gate length is 0.6μm. Of course, it is not what we expect. To ensure a set 0.1μm shapes, a symmetrical group of shapes is added, decreasing from 1.9 to 0.1μm as well (the nether half graph show in Fig. 2). Thus, as long as deviation occurs in vertical direction (smaller than 2μm), we can always obtain a 0.1μm overlapped shape in case of in horizontal direction, we can make one mask to cover the other one more than 2μm, therefore all horizontal deviation could be ignored.

Using above dual-exposure method, we are able to locate the specific positions of the MOSFETs wanted. For this purpose, a group of test patterns in both masks are planned. We compress the figures in Fig. 2 in vertical direction, by reducing the space between successive two lines to 2μm instead of 10μm. At last, we get a set of test patterns after duplicate them in horizontal direction.

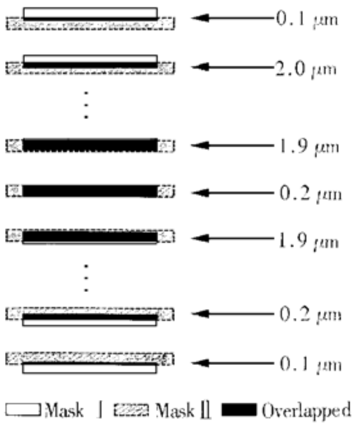

FIG. 2 Dual-Exposure Method

Besides getting small size devices in normal processing line, dual-exposure method has another merit. As we can see that, when 0.1μm MOSFETs are fabricated, a series of MOSFETs with different gate length are gained at the same time, which is quite meaningful for the device characteristics researches and parameter extraction. In addition, a relationship between the electrical characteristics and the channel length will be shown.

3 Physical and Electrical Test Results

We manufactured all samples on 2μm processing line. In practice, we not only use SiO_2-resist overetching or dual-exposure methods alone, but also the combination of them two. That is to say, use the dual-exposure method is used to get a series of MOSFETs with different gate lengths, then the polysilicon gate overetched with SiO_2-resist to reduce the gate length further. From the test results, we can draw a conclusion that this combination is very successful in obtaining MOSFETs series with gate length ranging from 0.1 to 1.9μm.

3.1 Physical Feature Test

First, we use test patterns to locate the probable 0.1μm MOSFETs. Then in physical feature test, we determine the actual gate and the channel length of MOSFETs by Scanning Electron Mocroscope(SEM). As a result, the smallest MOSFET we got has gate length of 0.12μm (see Fig. 3). To research the relationship between electrical characteristics and channel length, we select two more MOSFETs, whose channel lengths are 0.19μm and 0.25μm respectively.

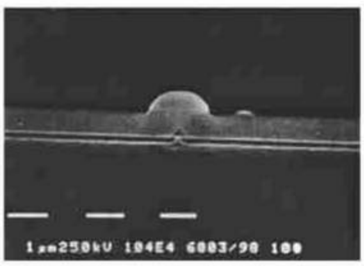

FIG. 3 0.12μm Gate Length MOSFET

3.2 Electrical Characteristics Test

The equipment used for electrical characteristics test is HP4061A test system. Test items include output characteristics and substrate currents[10]. Substrate currents are measured when V_{ds}= 4V. Fig. 4 to Fig. 7 are test results.

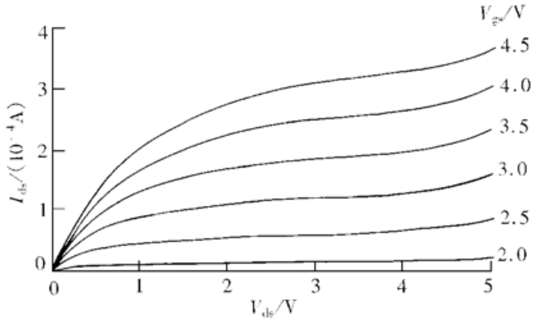

FIG. 4 Output Characteristic for 0.25μm MOSFET

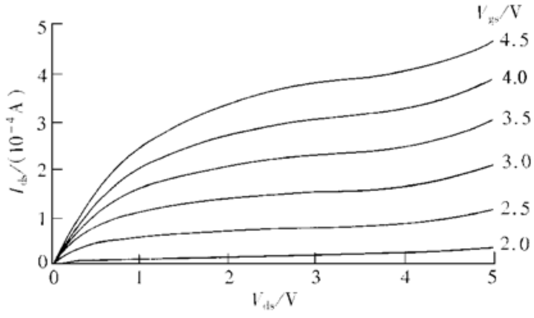

FIG. 5 Output Characteristic for 0.19μm MOSFET

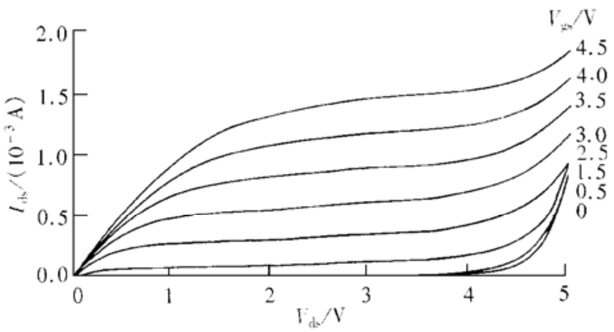

FIG. 6 Output Characteristic for 0.12μm MOSFET

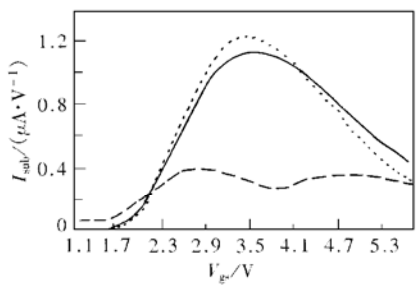

FIG. 7 Substrate Currents

4 Test Results Analysis

4.1 Source-Drain Output Saturation Currents(Fig. 8)

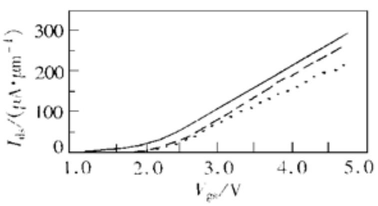

FIG. 8 S-D Saturation Currents

We extract the saturation currents from output characteristics at V_{ds} to be 4V. Data listed in Table 1 are unified to the saturation currents (μA) per μm width. From Table 1 and Fig. 8, we can see that I_{ds}(0.19μm) is 20% higher than I_{ds}(0.25μm), while I_{ds}(0.12μm) is 40% higher than I_{ds}(0.25μm). This indicates that the shorter the channel length is, the higher the output source-drain saturation currents will be.

Table 1 Saturation Currents per Micron Channel Width (A/ m) at V_{ds}= 4V

V_{gs}/V / L/μm	1.0	1.5	2.0	2.5	3.0	3.5	4.0	4.5
0.25	8.87×10^{-6}	0.3	12.5	44.9	87.3	132.2	177.3	220.0
0.19	1.87×10^{-4}	0.4	15.3	55.0	107.5	162.0	215.3	266.7
0.12	4.06	5.7	34.2	82.0	135.2	190.2	246.8	304.0

4.2 Transconductance

Again, on the basis of the extracted saturation currents from the output characteristics when V_{ds}= 4V, we calculated the transconductance(μS) of MOSFETs. Data from the Table 2 shows that G_m(0.19μm) is about 20% higher than G_m(0.25μm), and G_m(0.12μm) is about 30% higher than G_m(0.25μm). These results show that the transconductors increases while MOSFETs' channel length shrinks.

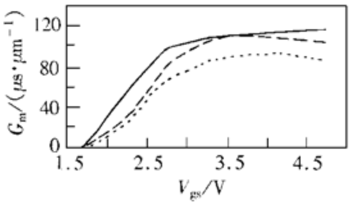

FIG. 9　Transconductance

Table 2　Transconductance per Channel Width (S/ m) at V_{ds}= 4V

L/μm \ V_{gs}/V	1.0	1.5	2.0	2.5	3.0	3.5	4.0
0.25	0.6	24.4	64.7	84.9	89.7	90.3	85.3
0.19	0.8	29.8	79.5	104.9	109.1	106.7	102.7
0.12	3.2	57.1	95.6	106.4	110.0	113.2	114.4

4.3 Substrate Current

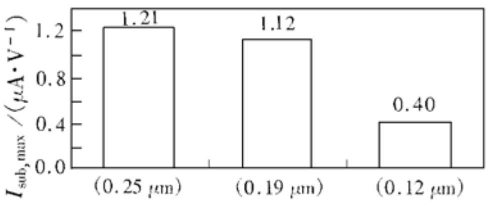

FIG. 10　Peak Substrate Currents

In substrate current analysis, we pick-up the maximum currents (μA) of MOSFETs(Fig. 10), and then unify them to the currents per micron channel width and per channel electric field intensity (V/μm). It is obvious from the bar graph that the substrate currents decrease when the channel length shrinks.

Table 3　Substrate Current per Channel Width per Electric Field Intensity

L/μm	$I_{sub,max}$/(μA·V^{-1})
0.25	1.21
0.19	1.12
0.12	0.40

This result on substrate current is quite exciting. In common opinion, the substrate currents will increase dramatically because of hot carrier effect[11] when channel length decreases, especially in deep submicron scale. Therefore, to prevent the devices from degrading, some extra techniques must be introduced, such as LDD structure[5], drain engineering[6] and channel engineering[7,8]. However, our results show that when MOSFETs' channel lengths enter 0.1μm scale, their substrate currents will decrease with the channel length shrinking. This could be attributed to the less collision probability for a single electron due to shorter moving path, and lower electron density in an inversion layer[2]. Thus, it would be suspectable whether special techniques are indispensable.

5 Conclusion

We have proposed two novel methods to manufacture 0.1μm MOSFETs in a micron scale processing line. These methods are verified in practical processing, in which the minimum channel length of 0.12μm is achieved. In addition, using dual-exposure method, we can make a series of MOSFETs with different gate length from 0.1 μm to 1.9 μm. This is quite meaningful to characteristics research and parameter extraction. Based on test results, the following conclusion could be drawn: within 0.1μm scale, when MOSFETs' channel length diminish, both saturation currents and transconductance increase, but substrate currents decrease.

References

[1] R.K.Watts, Submicron Integrated Circuits, reading, New York: Wiley.

[2] 曹建民, 吴传良, 沈文正, 等, 半导体学报, 1998, **19**(4): 280—286[CAO Jianmin, WU Chuanliang, SHEN Wenzheng *et al.*, Chinese Journal of Semiconductors, 1998, **19**(4): 280—286 (in Chinese)].

[3] 张文良, 田立林, 杨之廉, 半导体学报, 1999, **20**(2): 113—121[ZHANG Wenliang, TIAN Lilin and YANG Zhilian, Chinese Journal of Semiconductors, 1999, **20**(2): 113—121 (in Chinese)].

[4] 孙自敏, 刘理天, 李志坚, 半导体学报, 1998, **19**(11): 851—856[SUN Zimin, LIU Litian and LI Zhijian, Chinese Journal of Semiconductors, 1998, **19**(11): 851—856 (in Chinese)].

[5] Paul J., *et al.*, IEEE Transaction on Electron Devices, 1982, **ED-29**(4): 590—596

[6] Hiroaki Mikoshiba *et al.*, IEEE Transaction on Electron Devices, 1986, **ED-33**(1): 140—144.

[7] H.Tian *et al.*, IEEE Transactions on Electron Devices, 1994, **41**(10): 1880—1882.

[8] Jarvis B. Jacobs *et al.*, IEEE Transaction on Electron Devices, 1995, **42**(5): 870—875.

[9] Renate Sitle *et al.*, IEEE Transaction on Electron Devices, 1994, **41**(11): 2210—2215.

[10] 张锡盛, "用电荷泵法研究短沟 MOSFET 的热载流子蜕变效应", 清华大学博士论文[ZHANG Xisheng, Investigation of Damage of Hot-Carrier in Short Channel MOSFET by Charge Pumping, PH.D Thesis of Tsinghua University].

[11] Enrico Sangiorgi *et al.*, IEEE Electron Device Letter, 1988, **9**(1): 13—16.