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Improvement in Electrical Properties of SIMNI Films by Multiple-Step Implantation*

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Abstract: SOI-SIMNI (Silicon On Insulator-Separation by Implanted Nitrogen) films were formed with standard method and multiple-step implantation one. The Hall-effect measurements (4—300K) show that the multiple-step implanted SIMNI films have a lower sheet resistance and higher carrier mobility than those in standard SIMNI films. The DLTS results indicate that there is a deep level defect (E_t= 0.152 eV) in the standard SIMNI films but no such defects in the multiple-step implanted ones. The multiple-step implanted SIMNI films have good electrical properties.

Key words: electrical properties; multiple-step; implantation

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1 Introduction

In the past decade, there is an increasing interest in making Silicon-On-Insulator (SOI) films by high dose oxygen or nitrogen implantation into silicon, which will replace SOS (Silicon-On-Sapphire) to fabricate the high-speed, no latch-up CMOS circuits and the radiation hardened devices[1—4]. In this paper, we mainly report the fabrication of SIMNI films with two methods and their properties using the Hall-effect measurement and DLTS (Deep Level Transient Spectra). The Hall-effect measurements (4—300K) show that the multiple-step implanted SIMNI films have a lower sheet resistance $R_\square$ and higher carrier mobility than that in standard SIMNI films. The maximum mobility is $2.7\times10^4\ \mathrm{cm^2/(V\cdot s)}$ at 46 K in the former. The DLTS results indicate that there is a deep level defect (E_t= 0.152eV) under the conductive band bottom E_c in the standard SIMNI films but no one in

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the multiple-step implanted SIMNI films.

2 Sample Preparation

SOI-SIMNI wafers were made by using N^+ implantation at energy of 180keV, with dose of (1.1—1.2) $\times 10^{18}$ N^+/cm^2 into 10Ω·cm, n-Si <100> substrate at the implantation temperature T_i of 550—700℃, and then by annealling at the temperature T_a of 1200℃ for 2h (Standard Method). The sample SK2T was a standard SIMNI wafer. SK21T was a multiple-step implanted one, having been annealed in 5 steps in the implantation chamber at 1000℃ with 15min per step implantation. After the implantation, the wafer was annealed at T_a of 1200℃ for 2h.

3 Experimental Results

The thickness of SIMNI films was measured by interference spectra (IF) and spreading resistance (SR) method[5]. Table 1 is the thickness of the surface silicon layers d_{Si} and the buried Si_3N_4 layers d_{SN} by IF and SR method. We did the Hall-effect measurements (4—300K) using Van der Pauw method[6] with magnetic field of 0.32T and sample electrical current of 500μA. Four ohmic contacts were made in the corners of the

Table 1 Thickness d_{Si} and d_{SN} by IF and SR

No.	d_{Si}/nm IF	d_{Si}/nm SR	d_{SN}/nm IF	d_{SN}/nm SR
SK2T	248.7	260.0	174.5	160.0
SK21T	269.2	290.0	166.1	185.0

SIMNI square sample (see Figure 1). First, the 4 contacts areas were implanted phosphorous ions at 50 keV, $5\times10^{15}/cm^2$, then annealed at 900℃ for 15s. Second, In as a solder material was used to make the 4-electrode contacts and the 4 wires connected the contacts in a measurement chamber. From semiconductor physics, we knew

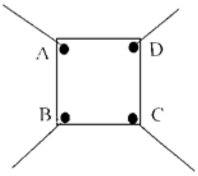

FIG. 1 SIMNI Square Sample

$$R_\square = \frac{\rho}{d_{Si}} = \frac{1}{ne\mu d_{Si}} \quad (1)$$

Where ρ and d_{Si} were the resistivity and thickness of the surface Si in SIMNI films; n, e and μ were the carrier (here electron) concentration, electron charge and carrier mobility, respectively. In the measurements, when the small current I_{AB}= 500μA passing through from contact A to B, let the voltage difference V_{DC} be $V_D - V_C$, then we obtained a resistance:

$$R_{AB.DC} = \frac{V_{DC}}{I_{AB}}$$

In the same way, we got:

$$R_{BC.AD} = \frac{V_{AD}}{I_{BC}}$$

Van der Pauw method[6] gave the following:

$$\rho = \frac{\pi d}{\ln 2}\frac{R_{AB.DC} + R_{BC.AD}}{2} f(R_{AB.DC}/R_{BC.AD}) \quad (2)$$

Where the correction factor f had relations with $R_{AB.DC}/R_{BC.AD}$:

$$\cosh\left[\frac{(R_{AB.DC}/R_{BC.AD}) - 1}{(R_{AB.DC}/R_{BC.AD}) + 1}\frac{\ln 2}{f}\right] = \frac{1}{2}\exp\left[\frac{\ln 2}{f}\right] \quad (3)$$

If the 4 contacts made in symmetry, $R_{AB.DC} = R_{BC.AD}$, $f = 1$, so the formula (2) became

$$\rho = \frac{\pi d}{\ln 2} R_{AB.DC} \quad (4)$$

From the formula (1) and (2) we had the formula:

$$R_{\square} = \frac{\pi}{\ln 2}\frac{R_{AB.DC} + R_{BC.AD}}{2} f(R_{AB.DC}/R_{BC.AD}) \quad (5)$$

In order to measure the Hall-coefficient R_H, let current I pass throuth the sample from A to C, we measured the voltage difference V_{BD} between contact B and D; while the magnetic field B_M was added to the surface of SIMNI film vertically, we measured the V'_{BD} and obtained the difference of Hall voltage ΔV_{BD} of $V'_{BD} - V_{BD}$. The Hall-coefficient was

$$R_H = \frac{d}{IB_M}\Delta V_{BD} = \frac{d}{B_M}\Delta R_{AC.BD} \quad (6)$$

Where $\Delta R_{AC.BD} = \frac{\Delta V_{BD}}{I}$. The mobility of the surface layer in SIMNI films was

$$\mu = R_H/\rho \quad (7)$$

Figure 1 is the sheet resistance derived from sample SK2T and SK21T as a function of temperature T. From Fig. 2, some conclusions can be drawn directly: (i) There is a minimum sheet resistance $R_{\square}$ due to the maximum mobility in both samples (see Fig. 3). (ii) In the multiple-step implanted sample SK21T, there is a lower sheet resistance $R_{\square}$ than that in the standard SIMNI sample SK2T. Because there is a higher mobility in SK21T surface Si layer than that in SK2T. Figure 3 shows the mobility μ as a function of temperature T. We can clearly observe: (i) The mobility of SK21T increases with the increase of temperature between 4—45K, μ-$T^{2.95}$, which belongs to the ionised donor scattering. (ii) The mobility decreases with the increase of temperature between 46—300K, μ-$T^{-2.55}$, which belongs to the lattice scattering and some others such as: electron, phonon scattering etc. (iii) The maximum μ_{max} equals to 2.7×10^4 $cm^2/(V \cdot s)$ at ~ 46K in sample SK21T. The maximum mobility is caused by two different scattering mechanisms (i) and (ii). (iv) The mobility of SK21T is much higher than that in SK2T. It means the surface silicon layer in multiple-step implanted sample (SK21T) has very good electrical properties because of its excellent crystal surface. DLTS measurements were carried out[5]. We did not find the DLTS defects in SK21T, but there is a DLTS defect level (E_t = 0.152 eV) in SK2T, which was calculated with DLTS method.

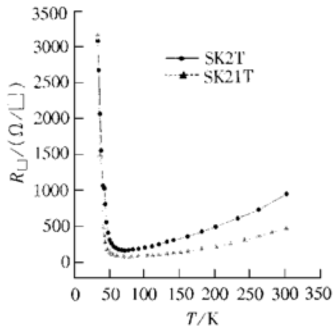

FIG. 2 Sheet Resistance $R_{\square}$ as Function of T from SK2T and SK21T.

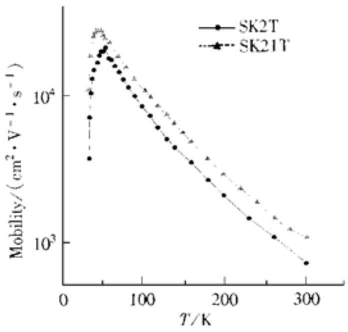

FIG. 3 Mobility μ as Function of T from SK2T and SK21T.

4 Conclusion

SOI-SIMNI wafers were formed with two different methods: the standard method and multiple-step implantation method. The mobility in SK21T (5-step implanted sample) is much higher than that in standard sample. The mobility of step-implanted SIMNI film is nearly twice of that of standard one. This indicates that taking multiple-step implantation and annealing is a good way to produce SIMNI films. The Hall measurement error is less than 3%. In the step-implanted SIMNI sample, the dose of every step implantation is less than the critical one, at which the amourphours layer is formed in the implanted silicon surface. Every annealing is a plus factor to reduce the surface damage caused by ion implantation and recovering the surface crystal lattice. We did not find the deep level defects in the surface silicon layers of step-implanted SIMNI sample. The DLTS results show that there is a deep level defect (E_t= 0.152eV) in silicon surface layers of standard SIMNI films. The DLTS measurement error is less than 5%. The multiple-step-implanted wafer (SK21T) has excellent electrical properties. With this method, the electrical properties of SIMNI films can be improved. Good electrical properties in SOI wafers, especially high carrier mobility, are very important for the fabricating of high-speed and radiation-hardened SOI/CMOS devices.

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