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Impact of Device Architecture on Performance and Reliability of Deep Submicron SOI MOSFETs (invited paper)

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Abstract: The main electrical properties of advanced Silicon-On-Insulator MOSFETs are addressed. The subthreshold and high field operations are analysed as a function of device architecture. The special SOI parasitic phenomena, such as the floating body potential and temperature, are critically reviewed. The main limitations of submicron MOSFET are comparatively evaluated for various SOI structures. Short channel and hot carrier effects as well as the reliability of the SOI technology are investigated for gate length down to sub-0.1 micron.

Key words: MOSFET; SOI; deep submicron; performance; reliability
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1 Introduction

A number of advantages, suitable for many applications, are obtained with the SOI structure which allows to push back the technological and physical limits intrinsic to the bulk Si structure[1,2,3]:

- the latch-up, a parasitic n-p-n-p structure (thyristor) which can be triggered in bulk silicon CMOS, is suppressed by the dielectric isolation of the Silicon-On-Insulator technology;

- ultra-thin SOI films, inducing a full depletion of the active silicon layer, can easily be fabricated and have been shown to lead to very interesting behaviors. In this respect, a low threshold voltage together with small leakage currents can be obtained which is of major importance for low power-low voltage integrated circuits used in portable electronic systems.

- the parasitic source/drain junction capacitances are substantially reduced using thin film SOI. leading to high frequency operation:

- the leakage currents are significantly smaller in SOI than that of bulk Si devices

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(2—3 order of magnitude) due to the reduction of the drain junction area;

- in the DRAM field, the SOI structure also lead to improved performances;
- SOI MOSFETs are of great interest for special applications, especially in the field of radiation hardness for both space and nuclear radiation environments;
- the SOI technology leads to new 《system on chip》 concepts;
- the special SOI structure can be advantageously used for developing new devices, like the volume-inversion MOSFET, the voltage-controlled bipolar MOS device, or quantum devices;
- some process simplification are induced by the SOI technology, mainly in the isolation and high energy implantation;
- three-dimensional IC's can also be realized on SOI materials, allowing a further potential enhancement of the level of circuit integration.

In view of the huge amount of work recently carried-out by many companies, it seems that the SOI CMOS technology is really taking off.

The aim of this paper is to give a review of the main advantages, drawbacks, performance and physical mechanisms of deep submicron SOI MOSFET. In this respect, the basic electrical properties (subthreshold swing, drain current), the special SOI phenomena (kink, parasitic bipolar, self heating), and the critical behaviors for advanced devices (short channel and hot carrier effects) will be thoroughly discussed.

2 Drain Current in Weak and Strong Inversion

Subthreshold Operation:

If the Fully Depleted (FD) SOI MOSFET is fabricated with a thick buried oxide and/or a low doping density in the silicon substrate (under the buried oxide) leading to small buried oxide and substrate (depletion) capacitances, the subthreshold swing S can be substantially lower than that observed in bulk devices. For small interface state densities at the various Si/SiO$_2$ interfaces, which is usually the case for present technologies, the swing can reach the minimum theoretical limit of about 60 mV/dec at 300 K[4]. This offers the opportunity to achieve both a low threshold voltage and a small leakage current. These fully depleted SOI devices are very interesting for high performances low voltage-low power integrated circuits.

The swing S for FD SOI MOSFETs can be described by[5]

$$S_{\rm SOI} = \frac{kT}{q}\ln(10)$$

$$\frac{(C_{\rm ox1} + C_{\rm ss1})[(C_{\rm si} + C_{\rm ss2})C + C_{\rm ox2}(C_{\rm sub} + C_{\rm ss3})] + C_{\rm si}[C_{\rm ss2}C + C_{\rm ox2}(C_{\rm sub} + C_{\rm ss3})]}{C_{\rm ox1}[(C_{\rm si} + C_{\rm ss2})C + C_{\rm ox2}(C_{\rm sub} + C_{\rm ss3})]} \quad (1)$$

where kT is the thermal energy, q the electron charge, $C_{\rm d}(=\epsilon_{\rm si}/x_{\rm d}$, $\epsilon_{\rm si}$ being the silicon permittivity and $x_{\rm d}$ the width of the depletion charge under the gate) the depletion capacitance, C_{ss}($= qN_{ss}$, N_{ss} being the interface state density) and C_{ox} the interface state and gate oxide capacitances for bulk structures, C_{si}($= \epsilon_{si}/t_{si}$, t_{si} being the Si film thickness) the thin Si film capacitance for SOI devices, C_{ox1} and C_{ox2} the gate oxide and buried oxide capacitances, C_{ss1}, C_{ss2} and C_{ss3} the interface state capacitances at the gate oxide/Si film, Si film/buried oxide and buried oxide/Si substrate interfaces, respectively, C_{sub} the substrate capacitance associated with the charge under the buried oxide, and $C = C_{ox2} + C_{ss3} + C_{sub}$.

The influence of the buried oxide thickness in a fully depleted SOI MOSFET is simulated in Fig. 1[5]. In the case of a thick buried insulator ($t_{ox2} \geqslant 300$nm), the swing is slightly reduced with decreasing the film thickness. In contrast, the swing shows a substantial increase with reducing the Si layer thickness in the case of a thin buried insulator (< 100nm). This behavior is observed for a high doping in the Si substrate inducing an accumulated buried oxide/silicon substrate interface (Figs. 1, 2). When the bottom surface of the buried oxide is depleted (for a low Si substrate doping), the substrate capacitance is significantly reduced. Therefore, the swing is improved with decreasing the film thickness whatever the buried oxide thickness is (Fig. 2), but the decrease of t_{ox2} always degrades the swing (Fig. 3).

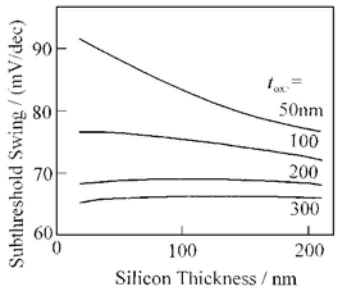

FIG. 1　Simulation of Subthreshold Swing as Function of Si Film Thickness for Various Back Insulator Thicknesses (gate oxide thickness $t_{ox1} = 27$nm, 10^{15} cm^{-3} Si film doping, $N_{ss2} = C_{ss2}/q = 0$, $N_{ss3} = C_{ss3}/q = 0$, accumulation at the buried oxide/Si substrate interface)

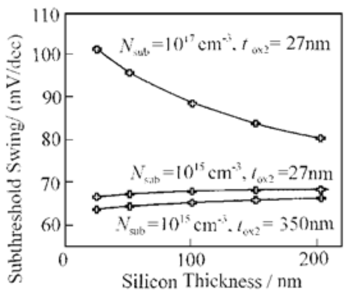

FIG. 2　Simulation of Subthreshold Swing as Function of Si Film Thickness for Various Back Insulator Thicknesses t_{ox2} and Substrate Doping N_{sub}($t_{ox1} = 27$ nm, 10^{15}cm^{-3} Si film doping, $N_{ss2} = 0$, $N_{ss3} = 0$)

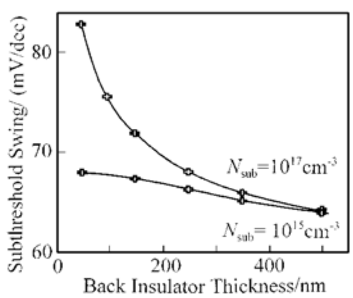

FIG. 3　Simulation of Subthreshold Swing as Function of Buried Oxide Thickness for Various Substrate Dopings ($t_{ox1} = 27$nm, 10×15cm^{-3} Si film doping, $N_{ss2} = N_{ss3} = 0$) Showing Degradation of Swing for Thin Buried Oxides

The back interface state density may also play a remarkable role. This is why for a Si film/buried oxide interface of poor quality ($N_{ss2} > 10^{11}$cm$^{-2}\cdot$eV^{-1}), the reduction of the silicon layer thickness does not lead to an improvement of the subthreshold swing (Fig. 4[5]). These results imply that the optimization of the device characteristics needs high-

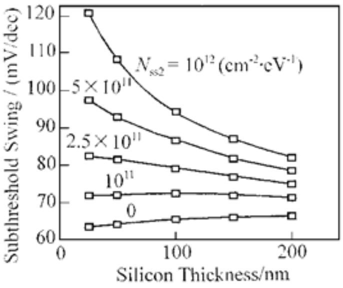

FIG. 4 Simulation of Subthreshold Swing as Function of Si Film Thickness for Various Back Interface State Densities ($t_{ox1}=27$nm, $t_{ox2}=350$nm, 10^{15}cm^{-3} Si film doping, 10^{15}cm^{-3} substrate doping, $N_{ss3}=0$)

quality SOI wafers as well as a careful design of the MOSFET parameters.

Driving Current in Advanced Devices:

In a fully depleted thin film SOI MOSFET, the transverse electric field is reduced as compared with a partially depleted film (for a given surface potential). This decrease is accentuated for thinner layers, the electric field having a quasi-linear variation with the Si film thickness. Therefore, the carrier profile extends deeper in the silicon film leading to higher carrier mobility μ owing to lower surface roughness and coulomb carrier scattering associated with the Si/SiO_2 interface. This interesting feature induces a substantial increase in drain current as compared to long channel bulk-like devices operated at same (V_g-V_t) bias ($I_{dsat}\propto(W/L)\,C_{ox}\mu(V_g-V_t)^2$, W and L being the gate width and length, C_{ox} the gate oxide capacitance). However, carrier velocity saturation driven by a high longitudinal electric field (the velocity maximum being v_{sat}) limits the current enhancement when the devices are scaled down in the deep submicron range ($I_{dsat}\propto W\,C_{ox}\,v_{sat}(V_g-V_t)$). The simulations presented in Fig. 5, fully supported by device measurements, show that the benefit of drain current, relative to bulk Si or Partially Depleted (PD) SOI, is partially lost as the channel length is reduced and carrier velocity saturation occurs[6]. However, in extremely thin Si layer (< 10nm), a substantial increase of the driving current with scaling down the devices has been pointed out in the deep submicron range. This effect is due to carrier velocity overshoot occurring in sub-0.1μm ultra-thin SOI devices[7].

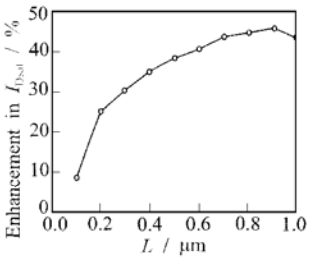

FIG. 5 Simulated Relative (to Bulk Counterparts) Enhancements of Drain Current in Saturation Versus Channel Length of Fully Depleted n-Channel SOI MOSFETs at $V_d=3.3$V and $V_g-V_t=1.7$V

3 Floating Body Effects

Kink Effect Analysis:

The buried insulator of the SOI structure leads to floating body effects. Indeed, contrary to the case of bulk silicon device, there is usually no substrate (or body) contact to determine the potential of the active Si layer and to collect free carriers induced by various mechanisms (for instance carriers created by impact ionization). When a body contact is available, the efficiency of this contact depends on the thickness of the Si film and on device architecture, owing to possible series resistance effect and/or potential barrier between the active silicon layer and the body contact.

The kink effect is one of the main floating body effects that are triggered by the impact ionization charging of the film body. It is observed in PD SOI MOSFET, and leads to excess drain current in saturation. The impact ionization in the high lateral electric field region close to the drain induces electron-hole pairs creation, the electrons flowing towards the drain and the hole forming the substrate current for a N-channel device. A reduction of the threshold voltage is obtained via the substrate current which leads to a forward bias of the source/Si layer diode and a body potential increase[8]. This phenomenon is also observed at low temperature in bulk silicon devices owing to impurity freeze-out in the Si substrate[9]. It has been shown that this parasitic behavior can be suppressed by using fully depleted devices[10].

The excess drain current ΔI_d and the shift of the threshold voltage ΔV_t[11] are given by

$$\Delta I_d = g_b V_b \tag{2}$$

where

$$g_b = \frac{C_d}{C_{ox}} g_m \tag{3}$$

$$\Delta V_t = -\frac{C_d}{C_{ox}} V_b \tag{4}$$

where $g_b (= dI_d/dV_b)$ is the body transconductance, V_b is the internal body potential induced by impact ionization, C_d and C_{ox} the depletion and gate oxide capacitances, respectively, and $g_m (= dI_d/dV_g)$ the gate transconductance.

For a fully depleted SOI MOSFET, the depletion capacitance C_d vanishes which suppresses the shift of the threshold voltage, the excess drain current and, thereby, the kink effect.

Thin film SOI transistors are subject to another harmful effect: the parasitic bipolar transistor. This last effect is enhanced with a reduction of the silicon film thickness (higher lateral electric field), especially for inversion-mode MOSFETs. An interesting trade-off could be the use of an intermediate Si layer thickness in order to suppress the kink effect and to alleviate the parasitic bipolar transistor action. Thin but undepleted SOI films were also proposed as an optimum substrate for low voltage CMOS[12]. However, it has been recently shown that a moderate kink effect can still be obtained for fully depleted SOI MOSFETs with intermediate Si film thickness (Fig. 6(a)[13]). This effect can be modulated by connecting the body terminal (Fig. 6(a)), if available. This kink is due to the substantial barrier height of the source/thin film diode in moderately fully depleted transistors.

In Figures 6(b), (c) are exemplified the transfer $I_d(V_g)$ characteristics for various applied body biases V_b. It is clear that the variation of the threshold voltage V_t from $V_b = 0$ to $V_b = -1$V, for a zero substrate voltage (Fig. 6(b)), is very small because the silicon film is already fully depleted for $V_b = 0$, and, therefore, the depletion region cannot be extend-

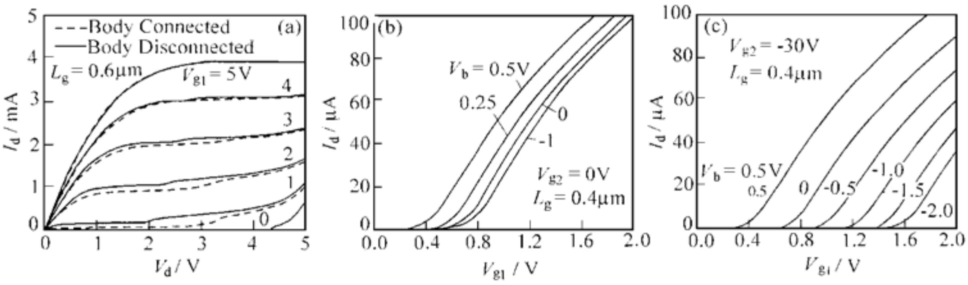

FIG. 6 (a) Output $I_d(V_d)$ Characteristics of n-Channel Thin Film SIMOX MOSFET Showing Influence of Body Connection; (b)-(c) Transfer $I_d(V_g)$ Characteristics Showing Influence of Body Bias V_b for Various Substrate Voltages V_{g2}

ed any more. On the other hand, with a small positive bias applied to the body terminal (up to 0.5V) a significant shift of V_t is obtained. In this case, the potential barrier between the source and the thin Si film can be reduced, due to the additional forward bias, because of its large initial value for this moderate full depletion. When a small positive substrate bias is applied (10V), the strong full depletion case is reached with a small potential barrier at the source/silicon film junction, which almost suppresses the variation of the threshold voltage for body voltages up to 0.5V. Finally, for a negative substrate bias, a large shift of V_t can be obtained for negative values of body voltages (Fig. 6(c)). This case corresponds to partially depleted SOI MOSFETs.

In moderately fully depleted devices, the depletion charge can be modulated for sufficiently large V_d, because of the possible change of the potential barrier at the source/substrate junction. The additional forward bias associated with the impact ionization current induces a reduction of the potential barrier and depletion charge; as C_d becomes different from zero (see Eqs. (2—4)), it gives rise to a small kink effect (which is in fact proportional to the reduced variation of the internal potential V_b close to the back interface). This reduced V_t shift has to be taken into account in order to obtain an accurate modeling of moderately fully depleted MOSFETs[13].

This means that these SOI MOSFETs are fully depleted for low drain biases, but for large drain biases, the devices become partially depleted, due to a reduction of the depletion charge. The physical difference between various devices is associated with the potential barrier at the source/substrate junction for small drain biases. The barrier is maximum for partial depletion, minimum for strong full depletion, and between these two extreme cases for a moderate full depletion which gives rise to a moderate kink. This kink effect can in fact be modulated by the degree of depletion of the Si film.

Parasitic Bipolar Action:

Another floating body effect is the Parasitic Bipolar Transistor (PBT) action which can be observed for SOI MOSFETs in a certain voltage range. This PBT induces latch and premature breakdown as compared to bulk Si devices[14]. As the kink effect, this parasitic phenomenon is triggered by the impact ionization current (base current) which leads to an internal forward bias of the (floating) base/emitter (thin Si film/source) junction of the PBT. A large collector (drain) current (base current × gain of the PBT) is thus created giving a substantial enhancement of the drain current. This PBT action portends power-consumption problems in SOI CMOS, hysteresis in the subthreshold characteristics and eventually the loss of gate control.

Breakdown and latch phenomena have been reported for both N- and P-channel enhancement- and depletion-mode devices[15—18]. For P-channel transistors, these effects are attenuated by the lower impact ionization rate of holes.

The latch and breakdown phenomena can also be improved by optimization of the device structure. For instance, lightly doped drain and source regions are useful in order to reduce the impact ionization near the drain (lower lateral electric field) and the gain of the PBT by maximizing the recombination in the source (emitter) region[16]. Another possibility is to fabricate a dual source SOI MOSFET[19], where the source region is an n^+ over p^+ structure (for N-channel), both regions being contacted by the same spiked aluminium electrode. In this transistor, the buried p^+ region collects the holes created by impact ionization near the drain, thus eliminating the PBT. In fact, this structure acts as a body contact without increasing device area. Other possibilities are the silicidation of the source region in order to decrease the gain of the PBT[20], bandgap engineering using a SiGe source[21], localized lifetime killing (away from the source and drain regions)[22], and reduction of the supply voltage if allowed by system constraints.

The latch and breakdown phenomena associated with the parasitic bipolar transistor action are temperature dependent. Figure 7 presents a typical off-state ($V_g = 0$) breakdown for a thin-film (80 nm) LDD SOI n-MOSFET as a function of temperature[18]. At 300K, a conventional breakdown is observed at low drain bias (< 4V), unlike at liquid nitrogen temperature where breakdown is avoided for V_d below 6V. Similar improvements are obtained for the latch phenomenon in the $I_d(V_g)$ characteristics. These considerable advantages at low temperature are attributed the variation of the gain of the bipolar transistor. Indeed, the PBT gain β decreases quasi-exponentially with reducing the temperature ($\beta \propto \exp(-\Delta E_g/kT)$), due to the difference in bandgap ΔE_g between emitter (source) and base (thin Si film).

For the same reason, at high tempature the bipolar action is substantially accentuated, leading to high gain and leakage current (Fig. 8[23]).

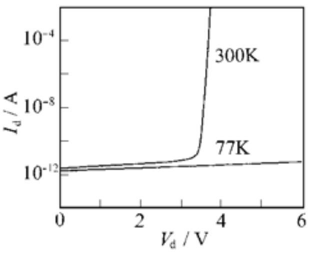

FIG. 7 Off-State Breakdown (V_g= 0) at 300 and 77K for n-Channel Thin-Film Depletion-mode SIMOX MOSFET (t_{si}= 80nm, W= 40μm, L_g= 0.8μm)

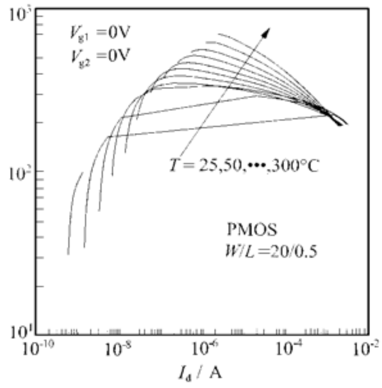

FIG. 8 Gain of Parasitic Bipolar Transistor as Function of Drain (Collector) Current for Various Temperatures up to 300℃

Noise:

Flicker noise in microelectronics devices, observed at low frequency with a variation inversely proportional to the frequency ($1/f$), is very harmful for analog applications. It is attributed to carrier mobility or carrier number fluctuations. When the drain current noise is proportional to the transconductance squared or inversely proportional to the drain current, it is concluded that the carrier number fluctuation model[24—26] or the Hooge mobility fluctuation model[27], respectively, is valid. In MOS transistors, the main fluctuations are due to dynamic exchange of channel carriers with interface or oxide traps (carrier number fluctuations).

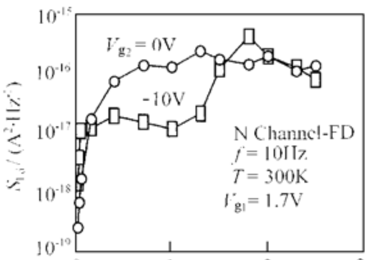

FIG. 9 Experimental Drain Current Noise as Function of Drain Voltage, for Various Back Gate Biases (N-Channel Thin Film (80nm) Enhancement-Mode SOI MOSFET) A Kink effect and an excess noise is obtained when the device is partially depleted (V_{g2}= - 10V).

In SOI MOSFETs, supplementary fluctuations are obtained owing to floating body effects. For a thin film fully depleted transistor, a conventional drain current noise (bulk-like) is obtained as a function of V_d (Fig. 9). However, when a negative bias is applied to the substrate (back gate), the device becomes partially depleted (accumulation of the back interface) and a kink effect is obtained leading to an excess noise around the kink (Fig. 9 with V_{g2}= - 10V)[28,29]. This excess noise can be attributed to the dynamic trapping of carriers created by impact ionization in the Si layer or at the interfaces of the SOI structure.

Another floating body effect, the parasitic bipolar transistor action which can be observed in both partially and fully depleted SOI MOS transistors, also leads to an original low frequency noise behavior. The noise measurements are shown in Fig. 10. For small drain current, below the threshold of the parasitic bipolar transistor, similar noise magnitudes are obtained for the various V_d values. However, for large I_d, the PBT regime is reached for a sufficiently high drain bias ($V_d \geqslant 3.3$V) leading to a significant increase of the noise. Similar results for the drain current noise are obtained in the case of forward-($V_d = 3.35$V) and reverse ($V_d = 3.3$V) -V_g-scan latch[30].

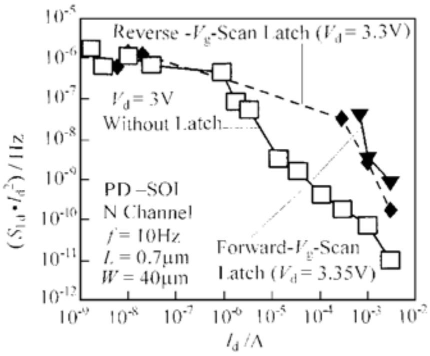

FIG. 10 Normalized Drain Current Noise vs Drain Current for N-Channel Partially-Depleted SOI MOSFET (t_{si} = 100nm, t_{ox1} = 4.5nm, t_{ox2} = 80nm) An excess noise is observed in the presence of both forward- and reverse-V_g-scan latch.

This excess noise is attributed to supplementary fluctuations associated with the impact ionization (generation) and carrier capture in the SOI layer (recombination). Note also that the impact-ionization current leads to a biasing of the base of the parasitic bipolar transistor, and further fluctuations can be caused by the PBT carrier transport between emitter (source) and collector (drain).

4 Self-Heating Effects

SOI MOSFETs suffer from self-heating effects conveyed by the low thermal conductivity of the buried oxide. At high power levels, one observes the onset of negative output conductance in the saturation region[31]. This behavior is mainly attributed to the reduction of the mobility with increasing channel temperature by Self-Heating (SH). However, other device parameters (threshold voltage, saturation velocity, etc.), have to be taken into account for accurate modeling. Self-heating also leads to an increase of the interconnect temperature which is critical for electromigration considerations. The excess temperature in the Si film can be expressed as

$$\Delta T = R_{th} I_d V_d \tag{5}$$

where R_{th} is the thermal resistance, and $I_d V_d$ the device power.

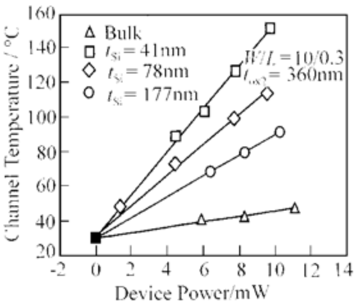

FIG. 11 Enhancement of Channel Temperature with Increasing Device Power for SOI Devices with Varying Si Film Thickness

Figure 11 shows the measured channel temperature versus device power for varying film thickness[32]. The temperature rise is proportional to the power, and is much larger in a SOI device than in a bulk Si transistor. As the silicon layer is thinner, the channel temperature substantially increases. The channel temperature is also raised with increasing the buried oxide thickness and the channel-metal contact separation[32]. The reduction of this important parasitic effect in SOI technology may require the device structure as well as the film and buried oxide thicknesses be optimized. Fortunately, reduced self-heating effects are obtained under dynamic operation.

A thorough analysis of this phenomenon has been carried out. Figure 12(a) shows typical output characteristics obtained for various back gate bias, V_{g2}, for a FD Unibond-SOI MOSFET (t_{Si}= 40nm, W/L= 25/0.8 μm/μm). In order to investigate the influence of the back-gate on the self-heating effect, the variations with drain voltage of the normalized drain current change $\Delta I_d/I_{dmax}$, which is expressed as $\frac{\Delta I_d}{I_{d\,max}}=\frac{I_{d\,max}-I_d}{I_{d\,max}}$, is shown in Fig. 12(b). Note that $\Delta I_d/I_{dmax}$ decreases when the back interface is accumulated ($V_{g2}< 0$ for N-channel). Indeed, in this partially depleted case, the threshold voltage V_t is more sensitive to temperature because of the possible variation of the maximum depletion charge. Then, when the self heating is accentuated, V_t decreases (higher temperature) which induces an improvement of the drain current (reverse self-heating effect) and compensates the carrier mobility reduction[33]. This feature is confirmed by 2D simulation and modelling.

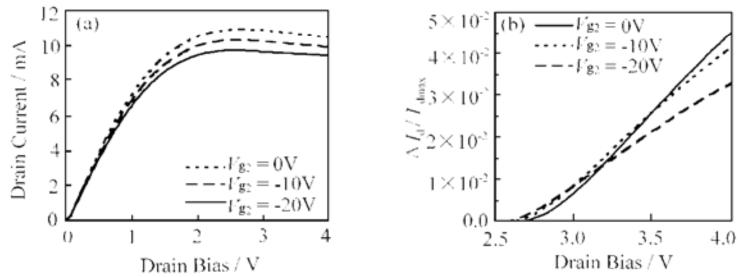

FIG. 12 (a) Typical Output Characteristics $I_d(V_d)$ and (b) Variations with V_d of Normalized Drain Current Change for Various Back-Gate Bias for N-channel Fully Depleted Unibond SOI MOSFET

Indeed, in Figure 13, the theoretical difference between I_{dsat} without self-heating and I_{dsat} with self-heating (ΔI_{d1}) is plotted versus the drain voltage for PD and FD devices, and also FD structure for which the Si-film becomes partially depleted at high temperature. In agreement with the experiment, the SH effect in PD SOI-MOSFETs is lower than that observed in FD ones. Moreover, with increasing temperature, a fully depleted structure may become partially depleted. In this case (FD-PD, Fig. 13), for a drain bias up to 3V, the $\Delta I_{d1}(V_d)$ characteristic is given by the FD structure, and for a upper drain voltage, the drain current is calculated by the PD device model which leads to a decrease of ΔI_{d1} compared with the FD model[33]. It is worth noticing that similar behaviors have been obtained by simulation using a 2D device simulator.

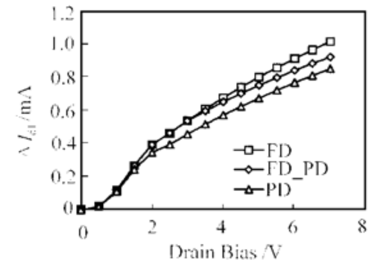

FIG. 13　Difference Between I_{dsat} Without SH and I_{dsat} with SH (ΔI_{d1}) vs V_d for PD ($N_a = 10^{18}\text{cm}^{-3}$, $V_g = 4\text{V}$), FD ($N_a = 7\times10^{17}\text{cm}^{-3}$, $V_g = 3.75\text{V}$) and FD-PD ($N_a = 7\times10^{17}\text{cm}^{-3}$, $V_g = 3.75\text{V}$) SOI Devices Obtained by the Analytical Model ($L_g = 0.7\mu\text{m}$, $W = 10\mu\text{m}$, $t_{si} = 40\text{nm}$, $t_{ox1} = 4.5\text{nm}$, $t_{ox2} = 380\text{nm}$)

For the fully depleted structure, the Si-film doping is the same as that for the FD-PD device, but in this last case the variation of the depletion charge with temperature is taken into account in the modelling.

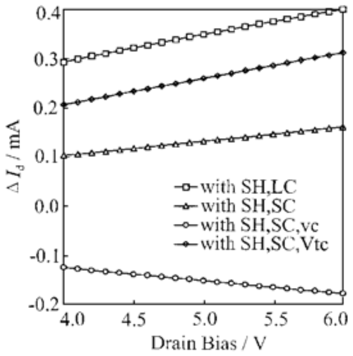

FIG. 14　Difference Between I_{dsat} Without Self Heating and I_{dsat} with Self Heating (ΔI_d) vs V_d for long ($L_g = 0.7\mu\text{m}$, $V_g = 3\text{V}$) and Short ($L_g = 0.1\mu\text{m}$, $V_g = 5\text{V}$) Channel Fully Depleted SOI Devices ($N_a = 10^{17}\text{cm}^{-3}$, $W = 10\mu\text{m}$, $t_{si} = 40\text{nm}$, $t_{ox1} = 4.5\text{nm}$, $t_{ox2} = 380\text{nm}$)

—□—With SH, LC: Long channel SOI MOSFET with self-heating effects

—△—With SH, SC: Short channel SOI MOSFET with self-heating effects

—○—With SH, SC, vc: Short channel SOI MOSFET with self-heating effects and taking into account a constant saturation velocity with temperature

—◇—With SH, SC, Vtc: Short channel SOI MOSFET with self-heating effects and taking into account a constant threshold voltage with temperature

Finally, in Fig. 14, the modelling of SH in short channels has been carried out by using the drain saturation current equation with the v_{sat} model used in the numerical simulation[34]. The saturation region is magnified for Long Channel (LC) and Short Channel (SC) SOI MOSFETs in Fig. 14 for which the difference between drain current without SH and I_{dsat} with SH (ΔI_d) is plotted versus the drain voltage. If a threshold voltage independent of temperature is taken into account in the modelling, a greater SH is found compared with a total dependence with temperature (It should be mentionned that the case of a constant V_t with temperature cannot be simulated with the 2D numerical simulation). In short channel devices as in long channel devices, the V_t variations tend to enhance I_{dsat} with increasing temperature. When v_{sat} is independent of temperature, a reverse SH is underlined ($\Delta I_d < 0$). Furthermore, SH effects in LC devices are greater than in SC ones owing to the variations of μ with temperature which are larger than the variations of v_{sat} versus temperature (Fig. 14). This trend is also in agreement with the numerical simulation[34].

5　Short Channel Effects in Various SOI MOSFET Architectures

Drain Induced Barrier Lowering (DIBL) and Charge Sharing (CS) effects, which are the main short channel phenomena, are calculated as follows: $\Delta V_t - \text{DIBL} = V_t(V_d = 0.05\text{V}) - V_t(V_d = 1.5\text{V})$ and $\Delta V_t - \text{CS} = V_t(L_g = 0.5\mu\text{m}) - V_t(L_g = 0.05\mu\text{m})$. Very impor-

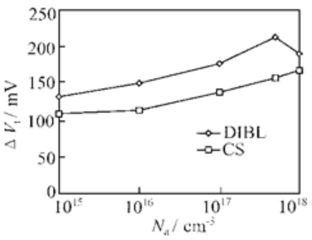

FIG. 15 DIBL and Charge-Sharing Effects as Function of Silicon Film Doping for 0.05μm SOI MOSFET (t_{si} = 10nm, t_{ox1} = 3nm, t_{ox2} = 380nm) ΔV_t - DIBL = V_t(V_d = 0.05V) - V_t(V_d = 1.5V); ΔV_t - CS = V_t(L_g = 0.5μm) - V_t(L_g = 0.05μm), V_d = 50mV, where L_g = effective gate length.

tant results are shown in Fig. 15 for 0.05μm SOI MOSFETs. The short channel effects (DIBL and charge sharing) are strongly improved with reducing the Si film doping down to very low concentration ($\leqslant 10^{16}$cm^{-3}). This behavior is very different from that observed in bulk Si devices for which large Short Channel Effects (SCE) would be obtained for such dopings in the sub-0.1μm range. The results of Fig. 15 are calculated for a 3nm gate oxide thickness and a 10nm Si film thickness. A further reduction of SCE can be obtained by thinning the gate oxide and/or the Si layer (see below). By using these very low doping concentrations, a dramatic reduction of the standard deviation of the threshold voltage due to doping fluctuations will also be obtained. Furthermore, in the case of ultra-thin Si films and very low dopings, large drain current and very small leakage currents for a drain bias up to 1.5V have been obtained for 0.05μm SOI MOSFETs. This device architecture allows to obtain a better control of the potential and charges in the active Si layer.

In SOI devices, it is also possible to use the substrate bias as a back gate. When the back Si film/buried oxide interface is accumulated, by applying a negative voltage on the back gate of a N-channel MOSFET, a substantial reduction of the DIBL effect is observed (Fig. 16). This accumulation of the back channel allows to enhance the potential control in the thin Si film, thereby improving the DIBL. For the charge sharing effect, the influence of the back channel accumulation is rather low (Fig. 17). Another possibility in SOI technology is the use of a double-gate control which induces a strong inversion in the whole silicon layer for thin film transistors (volume inversion). This double-gate control leads to a dramatic improvement in the DIBL and charge sharing effects (Figs. 16, 17). These advantages are obtained together with very large driving current and very small leakage currents for drain bias up to 1.5V in a wide Si film thickness range. For 0.05μm SOI MOSFETs, the short channel effects (DIBL and charge sharing) are reduced with decreasing the silicon film thickness (down to 5nm) whatever the architecture is (single gate and double gate (Figs. 16, 17)). Besides, a reduced dependence on the silicon film doping is observed for the double gate devices which is very interesting for the optimization of their electrical properties. It should be mentioned that energy quantization effects are neglected in our simulations because they are only significant for silicon film thicknesses lower than 5nm which is the limit of our investigations[35].

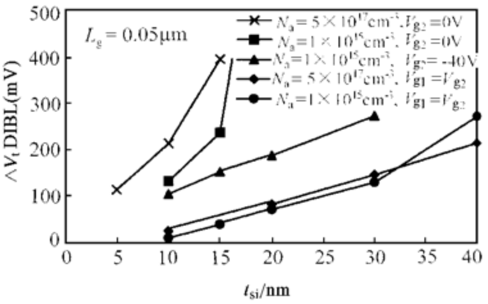

FIG. 16 DIBL Characteristics as Function of Silicon Film Thickness (t_{ox2}= 380nm, t_{ox1}= 3nm) for 0.05μm Single Gate SOI MOSFETs with High Doping (N_a= 5×10^{17}cm^{-3}, V_{g2}= 0V), Low Doping (N_a= 10×15cm^{-3}, V_{g2}= 0V), Back Channel Accumulation (N_a= 10^{15}cm^{-3}, V_{g2}= − 40V), and for Double Gate SOI MOSFETs (N_a = 10^{15}cm^{-3} and N_a= 5×10^{17}cm^{-3} with V_{g1}= V_{g2})

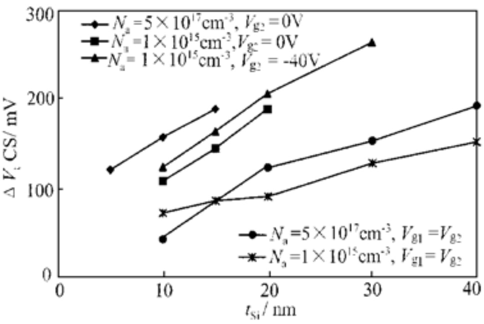

FIG. 17 Charge Sharing Effect Versus Silicon Film Thickness (t_{ox2}= 380nm, t_{ox1}= 3nm) for 0.05μm Single Gate SOI MOSFETs with High Doping (N_a= 5×10^{17}cm^{-3}, V_{g2}= 0V), Low Doping (N_a= 10^{15}cm^{-3}, V_{g2}= 0V), Back Channel Accumulation (N_a= 10^{15}cm^{-3}, V_{g2} = − 40V), and for Double Gate SOI MOSFETs (N_a= 10^{15}cm^{-3} and N_a= 5×10^{17}cm^{-3} with V_{g1}= V_{g2})

It is also worth noticing that the electron temperature is reduced with decreasing the Si film doping which is very interesting for long term device reliability[36]. The lowest electron temperature has been obtained in the case of a double gate SOI MOSFET.

6 Reliability of SOI Devices and Materials

The substrate current, the gate current or the number of emitted photon can be used for a reliable analysis of hot carrier effects in thin film fully depleted SOI MOSFETs. A substantial reduction of the normalized gate current is found for decreasing the Si film thickness. 1-D[3,38] and 2-D simulations (including the energy balance equation)[37] show that the inversion layer thickness increases with reducing the film thickness in fully depleted SOI transistors, which results in a decrease in the maximum electron temperature (Fig. 18)[37].

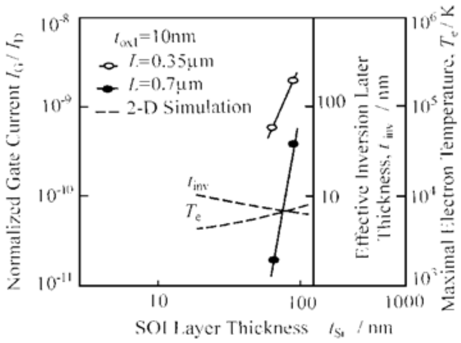

FIG. 18 Variation of Experimental Normalized Gate Current as Function of Si Layer Thickness Compared with Simulated Inversion Layer Thickness and Maximum Electron Temperature

Figure 19 shows the typical photon emission characteristics for a 0.1μm thin film N-channel SIMOX MOSFET (measurements with Hamamatsu hot-electron analyser PHEMOS-50). For a drain bias lower than 2.5V, a conventional bell-shaped curve is obtained as a function of gate bias, as in the case of substrate current characteristics. However, for higher V_d, a substantial enhancement of the photon number N_{ph} is observed for low V_g[39]. This behavior is correlated with the threshold of the parasitic bipolar transistor (PBT) which is triggered by impact ionization charging of the film body and can induce a latch phenomenon (loss of gate control). In Fig. 20 is presented the variation of N_{ph} versus V_g for various gate lengths (V_d= 2.5V). For the shortest SOI MOSFETs (L_g= 0.1 and 0.075 μm) the PBT regime is reached leading to a maximal photon emission for the lowest gate voltage, unlike the case of longer devices with a traditional bell-shaped curve[39].

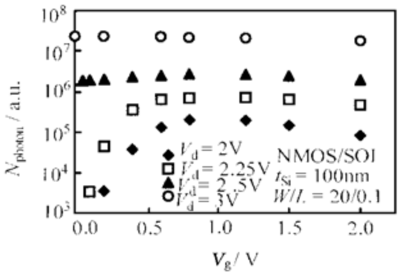

FIG. 19 Gate Voltage Dependence of Photon Number N_{ph} for Various Drain Biases for a 0.1 μm N-Channel SIMOX MOSFET

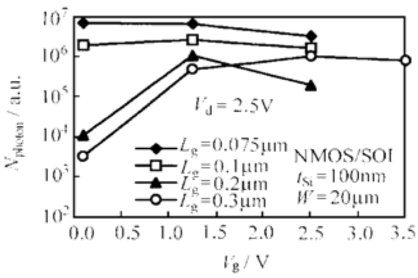

FIG. 20 Gate Bias Dependence of Emitted Photon Number as Function of Gate Length (V_d= 2.5V, N-Channel SIMOX MOSFET)

The typical degradation of the maximum transconductance after 10000s stress with various biasing conditions is shown in Fig. 21 for a 0.1μm gate length NMOS device. For $V_d \geqslant 2.5$V, the transistor aging increases with reducing the gate voltage, the maximal variation being obtained for V_g= 0. For a lower drain bias (V_d= 2V), the worst case is observed for V_g= $V_d/2$[39]. These results are in agreement with those obtained with photon emission measurements (Figs. 19, 20), and are due to the impact of the parasitic bipolar transistor as a function of the applied voltages.

The influence of the gate length is exemplified in Fig. 22 for N-MOSFETs. The maximal aging is reached for the lowest gate voltage in the 0.1μm range, while the worst case is obtained for intermediate value of V_g for longer devices (similar variations of V_t have been observed for V_d= 2.5V)[39]. These results are in full agreement with those of photon emission (Fig. 20).

In order to find a reliable lifetime evaluation of the MOSFETs, the time-dependent degradation laws have been thoroughly investigated. In previous works, many studies have been performed for bulk devices but no detailed analysis has been previously presented in the case of SOI MOSFETs. Figures 23 and 24 show the typical time-dependent degradation for the maximum transconductance of a 0.1 μm P-channel SIMOX MOSFET. Two regimes are clearly highlighted in these figures, a power time-dependent law for a short degradation time and a logarithmic time-dependent law for longer degradation time. This behavior is obtained both for a stress in the maximum substrate current (V_g= $V_d/2$, Figs. 23, 24) and in the maximum gate current conditions. Similar laws are underlined in the case of V_t shift and are obtained for both $V_g = V_d/2$ and $V_g = V_d$ conditions as well as for N-channel transistors[39].

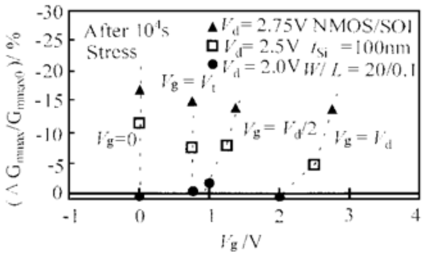

FIG. 21　G_{mmax} Degradation (in Linear Operation) as Function of Stress Gate Bias with Stress Drain Voltage as Parameter (10000s Stress, NMOSFET/SIMOX, W/L= 20/0.1)

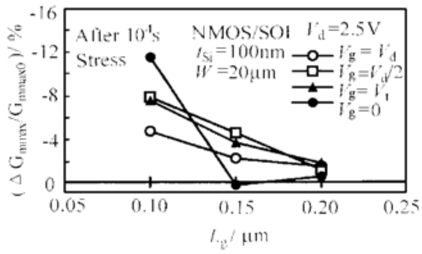

FIG. 22　G_{mmax} Degradation Versus L_g with Stress Gate Bias as Parameter (V_d= 2.5V, Stress Time= 10000s, N-Channel MOSFET/SIMOX, W= 20μm)

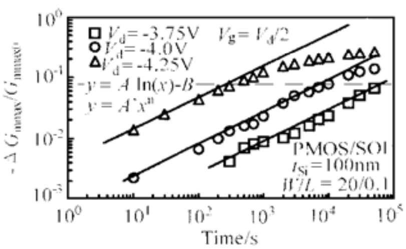

FIG. 23　Log-Log Plot of G_{mmax} Degradation vs Stress Time with Stress Bias as Parameter ($V_g = V_d/2$) for PMOSFET Showing Power Law

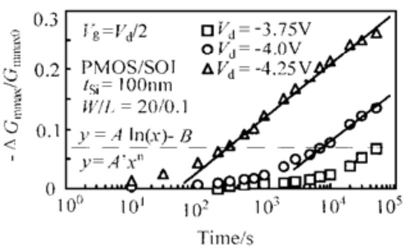

FIG. 24　Semi-Log Plot of G_{mmax} Degradation vs Stress Time with Stress Bias as Parameter ($V_g = V_d/2$) Showing Logarithmic Law

These various laws are used to calculate the maximum applied drain biases in order to obtain a 10 years lifetime (V_{dmax}) with various conditions (Fig. 25). V_{dmax} defined for G_{mmax} degradation= 10% is enhanced with increasing the channel length (Fig. 25(a)). V_{dmax} defined by ΔV_t= 100mV shows an original variation with scaling down the devices (Fig. 25(a)). It raises with increasing the channel length for L_g= 0.2μm (in the regime of the logarithmic law), and slightly decreases from L_g= 0.2μm to 0.3μm owing to the change of the time-dependent law. It should be mentioned that V_{dmax} for L_g= 0.4μm is almost equal to that of L_g= 0.2μm. A strong difference of V_{dmax} is obtained between the two definitions of the lifetime (G_{mmax} or V_t degradation) in the case of long channel devices. On the other hand, this difference is very small in the 0.1μm range[40].

The comparison between a degradation at $V_g = V_d/2$ and V_g= 0 shows that the worst case is obtained in the parasitic bipolar regime ($V_g \sim 0$) only for gate lengths larger than

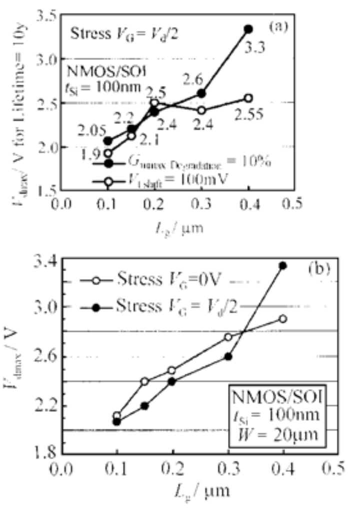

FIG. 25 Gate Length Dependence of Drain Voltage to Obtain 10 Years Lifetime (a) from G_{mmax} Degradation= 10% and ΔV_t = 100mV for N-Channel SOI MOSFETs (Stress $V_g= V_d/2$), (b) from G_{mmax} Degradation and a Comparison Between a Stress at $V_g= 0$ and $V_g= V_d/2$.

0.3μm (Fig. 25(b)). Therefore, the BPT action is not harmful for MOSFETs in the 0.1μm range.

Another important issue is the choice of the SOI material for the fabrication of ULSI circuits. Two major SOI materials, the SIMOX one (obtained by oxygen implantation at high dose and energy - or medium dose which gives the so-called《low dose SIMOX》) and the Unibond one (realized by the smart-cut® technique which combines both hydrogen implantation and wafer bonding), have been studied. Stresses during the back channel operation are performed for both FD Unibond and SIMOX devices in order to directly compare the BOX quality (Fig. 26). A similar G_{mmax} degradation is obtained for two devices, but the V_t shift of NMOS/Unibond is very small in both oxides as compared to that of SIMOX transistors. Consequently, Unibond MOSFETs have higher hot-carrier immunity than SIMOX ones[41,42].

7 Conclusion

The performances and physical mechanisms in deep submicron SOI MOSFETs have been thoroughly investigated. It has been shown that the the subthreshold operation and the driving current can be significatively improved by using the flexibility of the SOI structure as compared to bulk technology. The main special floating body phenomena have also been critically reviewed and solutions for reducing these parasitic effects have been given. For the ultimate integration of silicon, down to deep sub-0.1μm gate length, the substantial reduction of short channel effects in ultra-thin film and/or double gate SOI devices is a key advantage. Finally, it has been pointed out that the long-term reliability of SOI transistors can also be optimized.

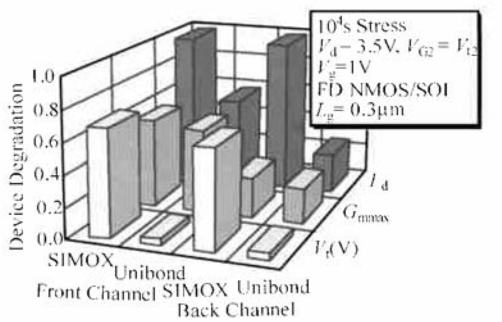

FIG. 26 Comparison of Device Aging Between FD SIMOX and FD Unibond N-MOSFETs
Stress performed during back channel operation. V_t shift was measured with depleted opposite interface.

Acknowledgments

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Biography

Francis Balestra was born in Digne, France, in 1960. He received the B.S. degree from the University of Provence, Marseille, France, in 1981 and the M.S. and Ph.D. degrees in electronics from the Institut National Polytechnique, Grenoble, France, in 1982 and 1985, respectively. In 1989, he obtained the Habilitation diploma from the INPG authorizing him to supervise Ph D. Dissertations.

He joined the Laboratoire de Physique des Composants à Semiconductures (LPCS), INP Grenoble, in 1982, where he has been involved in research on the characterization, modeling and simulation of fully depleted silicon-on-sapphire MOS transistors.

He became Chargé de Recherche C.N.R.S (Centre National de la Recherche Scientifique) in 1985. In 1993-94, he joined the Research Center for Integrated Systems at Hiroshima University as a visiting researcher, and worked on sub-0.1μm MOSFETs and thin film SIMOX devices.

Between 1996 and 1998 he has been Deputy Director of the LPCS, and he is Director of the LPCS since January 1999.

He led several research teams on deep submicron CMOS, silicon on insulator devices, low temperature electronics and polysilicon emitter bipolar transistors for BiCMOS technology. He has supervised 15 research projects and 17 Ph.D. He is presently coordinating and European project (ESPRIT Working Group 《Ultimate Integration of Silicon》) and a project supported by the Rhône-Alpes region 《Silicon Nanoelectronics》. He was the organizer of the first European Workshop On Low Temperature Electronics (WOLTE), Grenoble, France, June 1994 and of the first European Workshop on Ultimate Integration of Silicon (ULIS' 2000), Grenoble, France, January 2000.

Dr. Balestra has coauthored over 80 publications in international scientific journals and 120 communications at national and international conferences (20 invited papers and review articles).