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Numerical Analysis of Characterized Back Interface Traps of SOI Devices by R-G Current*

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Abstract: Characterized back interface traps of SOI devices by the Recombination-Generation (R-G) current has been analyzed numerically with an advanced semiconductor simulation tool, namely DESSIS-ISE. The basis of the principle for the R-G current's characterizing the back interface traps of SOI lateral $p^+ p^- n^+$ diode has been demonstrated. The dependence of R-G current on interface trap characteristics has been examined, such as the state density, surface recombination velocity and the trap energy level. The R-G current proves to be an effective tool for monitoring the back interface of SOI devices.

Key words: recombination-generation current; interface traps; SOI

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1 Introduction

SOI technology is based on the complicated fabrication process of ultra-thin silicon film on SiO_2 insulation layer. The key of improving the performance of SOI-based devices and circuits is to reduce the density of electron-hole recombination and trapping centers at the SiO_2-Si interface, with the purpose of suppressing the leakage current and improving the hot carrier reliability and radiation hardness.

Electronic traps at the SiO_2-Si interface are traditionally studied using the MOS capacitance[1-2], conductance[3] method on MOS capacitor, subthreshold, DLTS, PL, and have recently been characterized by Charge-Pumping-based method(CP)[4-7]. However, as the dimension of the SOI device is scaled into a sub-0.1 micrometer regime and the front- and

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back-gates of SOI devices are coupled each other, the conventional methods are demonstrated to be insensitive and inapplicable.

Recently, there exists an increased interest in the old gated-diode technique, to which, some new modifications are used to study the current bulk CMOS and SOI devices. Taking the advantage of high sensitivity and fast evaluation[8—12], the Recombination-Generation (R-G) current is reported to be an effective monitor characterizing the interface traps and bulk carrier lifetime.

However, in comparison with the conventional concrete R-G current measurements of SOI devices, only a little effort has been made to analyze the basic principle of this method. Our numerical analysis of the electrical characteristics of the interface traps with R-G current method has not been presented so far. In fact, interface trap effects on the R-G current have not been investigated in detail, neither has the influence of the front/back interface coupling on the R-G current.

The aim of this work is to obtain a comprehensive knowledge of the gated-diode R-G current through numerical simulation. Based on the similar SOI lateral gated-diode configuration with a slight forward bias, the R-G current of the back interface traps of SOI device is simulated by the advanced semiconductor simulation tool, namely DESSIS-ISE. Effects of the interface density, energy level, surface recombination velocity (SRV or S) and diode biasing voltage on the R-G current have been discussed in details.

2 Structure and Principle

The device used in this study is a common SOI lateral gated-diode structure, as shown in Fig. 1. The channel length is chosen as 10μm in order to enlarge the effect of the interface traps. The used structure parameters of the device are given in Table 1.

Please note that the default parameters used in the simulation should be the values in the table unless the especial note is given.

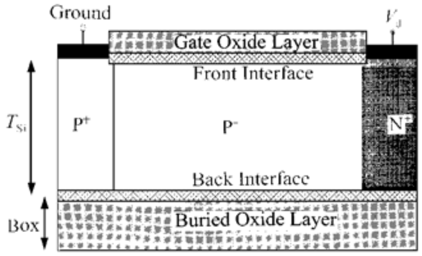


FIG. 1 Cross-Section of SOI Lateral Gated-Diode

Table 1 Parameters Used in Simulation

Parameter	Value	Type
N^+ or P^+ Concentration/cm^{-3}	1×10^{20}	Uniform
P^- Concentration/cm^{-3}	1×10^{17}	Uniform
Silicon Film Thickness/nm	80	
Gate Oxide Thickness/nm	10	
Buried Oxide Thickness/nm	300	
Back Interface Density/cm^{-2}	5×10^{11}	Single-Level
SRV or S/(cm · s^{-1})	20	
Interface Trap Energy Level/eV	0.01	From Midgap
Diode Biasing Voltage/V	−0.4	

It is known that dominance of the recombination via the defect levels in defected region is of particular importance, which is governed by SRH statistics[13].

On the surface or interface, the recombination rate R_{sur} for a single defect energy level at energy E_{trap} is

$$R_{\mathrm{sur}} = \frac{np - n_i^2}{\dfrac{n_1 + n}{S_{\mathrm{p0}}} + \dfrac{p_1 + p}{S_{\mathrm{n0}}}} \tag{1}$$

with

$$n_1 = n_i \exp\left(\frac{E_{\mathrm{trap}} - E_i}{kT}\right) \qquad p_1 = n_i \exp\left(-\frac{E_{\mathrm{trap}} - E_i}{kT}\right)$$

where E_i is the intrinsic Fermi energy, S_{p0} and S_{n0} are the electron and hole SRV parameters, respectively.

In general, electrons and holes can be assumed to be of the same SRV. The electron SRV parameter is defined as

$$S_{\mathrm{N0}} = N_{\mathrm{trap}} c_n \tag{2}$$

where c_n is often written as the product of the electron thermal velocity and the capture cross-section. N_{trap} in cm^{-2} is the density of the back interface traps. An analogous expression holds good for the hole.

The values of the carrier concentration n and p in the equation (1) should satisfy

$$np = n_i^2 \exp^{q\Phi/kT} \tag{3}$$

where Φ is the separation of the electron and hole quasi-Fermi levels (which is a functin of the position and the applied bias).

In the gated-diode case, the surface potential at SiO_2-Si interface and thus the surface excess carrier concentration are not only the function of the biased voltage V_d, but also that of the front and back gate bias voltage V_G. The interface R-G current can be expressed as

$$I_{\mathrm{R-G(sur)}}(V_d, V_G) = qw \int_{x_1}^{x_2} S F(V_G, V_d)\,\mathrm{d}x \tag{4}$$

with

$$F(V_G, V_d) = \frac{n(V_G, V_d)\,p(V_G, V_d) - n_i^2}{n(V_G, V_d) + p(V_G, V_d) + 2n_i}$$

where x_1 and x_2 are the boundaries of the space charge region. w is the depletion region´s thickness.

The total diode current is the sum of the interface R-G current $I_{\mathrm{R-G(sur)}}$, bulk R-G current $I_{\mathrm{R-G(bulk)}}$ and the bulk diffusion current $I_{\mathrm{diffusion}}$ for all bias states.

$$I_{\mathrm{tot}} = I_{\mathrm{R-G(sur)}} + I_{\mathrm{R-G(bulk)}} + I_{\mathrm{diffusion}} \tag{5}$$

In this simulation, we assume that the bulk traps of SOI device can be neglected in order to emphasize the influence of the interface trap. The interface R-G current is always dominant in either the forward or reverse state at a small bias voltage ($V_d < -0.5\mathrm{V}$). The measured diode current strongly depends on the voltages of the back gate and the front one.

When the diode bias voltage keeps constant but the gate voltage shifts the inversion threshold and gets through the depletion into an increasingly strong accumulation, the interface potential and thus the surface excess carrier concentration will be greatly changed. As a result, the diode diffusion current will keep constant, but the R-G current slowly increase first till a peak value at the condition below, then decrease, and finally, keep constant, too. As shown in Eq. (1), the maximum R-G current, calculated when $\frac{\partial R_{\mathrm{sur}}}{\partial n} = 0$, is obtained by

$$S_{\mathrm{n0}}n = S_{\mathrm{p0}}p = Sn_{\mathrm{i}}\exp\left(\frac{qV_{\mathrm{d}}}{2kT}\right) \tag{6}$$

and expressed as

$$I_{\mathrm{R\text{-}G(sur)}} = qR_{\mathrm{max(sur)}}wL_{\mathrm{si}} \tag{7}$$

with

$$R_{\mathrm{max(sur)}} \cong Sn_{\mathrm{i}}\exp\left(\frac{qV_{\mathrm{d}}}{2kT}\right)$$

Obviously, the magnitude of the peak R-G current is always proportional to the interface density and the SRV. The R-G current can be used as an indicator to show the characteristics of the interface traps. In practice, it is very difficult to characterize the back interface traps in SOI devices, due to the large thickness of the oxide layer in the back interface. Therefore, we investigate their characteristics numerically by R-G current in this work.

3 Results and Discussion

For the sake of simulation, we choose the back interface trap density, SRV and defect energy level as the variable, respectively. Using a 2-D numerical simulation tool, DESSIS-ISE[14], SOI device behavior can be thoroughtly observed. The main physical models used in the simulation are summarized in Table 2. Considering the low-voltage measurement and the static characteristics, the device heating-effect can be neglected and thus the drift-diffusion model is used. In order to screen the effect of the front interface on the diode R-G current, the voltage of the front gate should keep -2V to avoid its effect on the R-G current.

Table 2 Models Used in Simulation

Recombination Models	Mobility Model	Gate Current Models	Transport Model
- Tunneling - Auger - SRH - Band2Band	- Doping Dependence Phumob Enormal	- Fiegna - Fowler	Diffusion-Drift

The principle of the gated-diode interface R-G current has been discussed. As expected, the interface R-G current show a strong peak value under different diode bias condition, as shown in Fig. 2. It can be seen that the diode current rises and drops exponentially with the deviation of the back gate voltage from the intrinsic Fermi level, as well as the good symmetry of the R-G current along the scanning back gate voltage axis.

Of all interface trap parameters, the average interface density N_{it} is the most important one. In this simulation, we assume a uniform interface profile in the interface layer to simplify the mesh design. The simulation result is shown in Fig. 3.

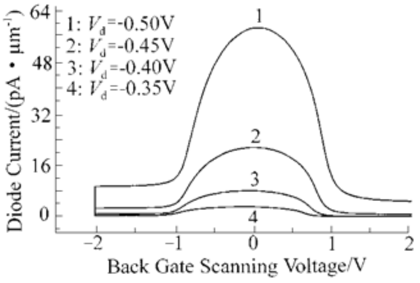


FIG. 2 R-G Current as Function of Back Gate Voltage at Different Diode Biasing State

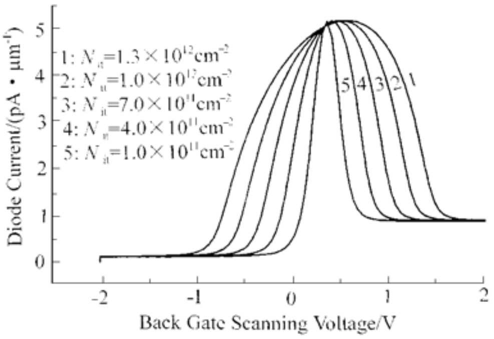
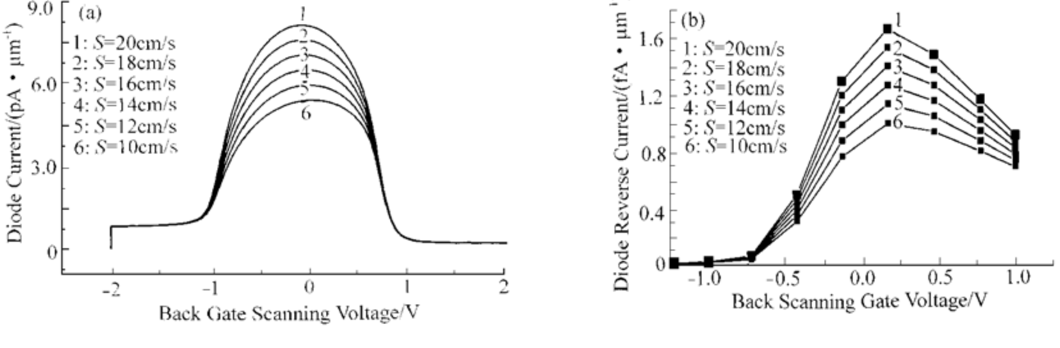


FIG. 3 R-G Current as Function of Back Gate Voltage for Different Interface Traps Density

It indicates that with the interface traps density increasing, the R-G current peak becomes higher, and the R-G current peak scatters do wider. Should be all trap energy levels assumed to located in the midgap level and have the same surface recombination velocity, the density value can be directly extracted from the magnitude of peak R-G current. However, it is only the first-order estimation.

Figure 4 shows the diode current characteristics at different surface recombination velocity (S) under the same bias voltage V_d, with one S being forward and the other reverse. It is obvious that the R-G current has a strong dependence on S no matter it is forward or reverse. Furthermore, the diode's forward current is observed to be approximately three orders magnitude higher than the reverse one under the same interface conditions.



(a) Forward Bias

(b) Reverse Bias

FIG. 4 Forward and Reverse R-G Current Characteristics of SOI Gated-Diode with Same Interface Trap Parameters

Let us consider the difference between the reverse and forward biasing lateral diode at a small V_d. Only generation processes via midgap states occur in the reverse bias, as reported in the former publication[9]. This generation current as a function of the gate and diode bias voltage can provide with the information about the interface traps.

In contrast, biasing the lateral diode in the forward mode, the current consists of two components in the depletion region, i. e. diffusion current and interface recombination current. For small forward biases, the recombination current is dominant and also to be a density monitor of the interface recombination centers. However, the relative change in the current of the forward mode is greater than that of the reverse one under the same interface condition and also easier to be measured.

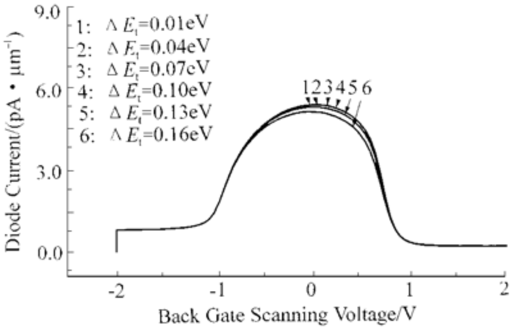


FIG. 5 I-V Characteristics of SOI Gated-Diode with Different Trap Energy Level

In order to prove the effect of the profile of interface trap energy level, Figure 4 shows the simulated R-G current result with different interface trap energy levels from midgap. Proven by theoretical analysis[15], the deviation of the defect energy level from the midgap has little effect on the recombination current unless it approaches the valence or the conduct band edge. From Fig. 5, it is found that the R-G current has almost the same magnitude if the differences between the interface traps and the midgap are less than 0. 1eV. If the deviation of interface traps level from the midgap is beyond 0. 1eV, the change of the R-G current is still very small.

It is well known that there exists a strong coupling between the back gate and the front one in the SOI device, whose effect is very difficult to distinguish. In the configuration of the SOI lateral gated diode, the R-G current can be used as a sensitive tool for demonstrating the coupling effect, as shown in Fig. 5.

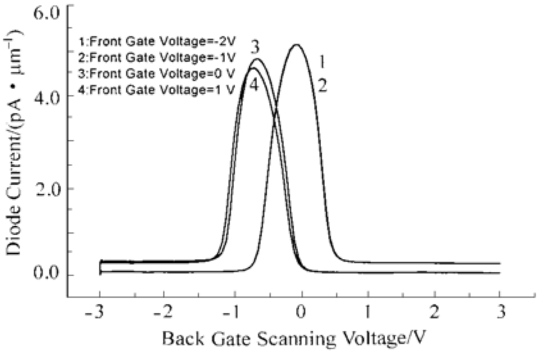


FIG. 6 Coupling Effect of Back Gate and Front Gate on R-G Current of SOI Gated-Diode

The R-G current is always in the single peak shape, with the peak position shifting significantly with the front gate voltage due to the interface coupling effect. It is believed that both the front and back gate interface traps can be detected individually and the coupling effect can be further analyzed based on the combination of the front gate voltage and the back gate one.

It should be pointed out that the R-G current method depends on the diode bias voltage. When the amplitude of the forward voltage V_d increases, the diffusion current will be dominant, and the R-G current method will become insensitive and imapplicable, which is only a small fraction the total current after all. Conventionally, the amplitude of the diode forward bias voltage for the R-G current method is less than 0.6V.

4 Conclusion

In this paper, characterized SOI back interface trap by R-G current method has been analyzed numerically. Using the simulation tool, DESSIR-ISE, the R-G current of SOI lateral $p^+p^-n^+$ diode with slight forward bias has been studied. The relationship between the R-G current and the interface characteristics such as the interface trap density, surface recombination velocity and trap energy level has been revealed.

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References

[1] A. Pacelli, A. L. Lacaita and S. Villa, IEEE Electron Device Lett., 1998, **19**: 148—150.

[2] C. H. Ling, S. E. Tan and D. S. Ang, IEEE Trans. Electron Devices, 1995, **ED-42**: 1321—1328.

[3] E. Nicollian and G. Goetzberger, Bell. Syst. Tech. J, 1967, **46**: 1055—1066.

[4] Tahui Wang, Lu-ping Chiang, Nian-kai Zous *et al.*, IEEE Trans. Electron Devices, 1998, **ED-45**: 1792—1796.

[5] Chin Hsin Wang and Arnost Neugroschel, IEEE Trans. Electron Device, 1992, **ED-39**: 662—670.

[6] Qin Guo-gang, Zhang Yu-fang, Du Yong-chang *et al.*, Chinese Phys., 1982, 820—824.

[7] Thierry Ouisse, Sorin Cristoloveanu, Tarek Elewa *et al.*, IEEE Trans. Electron Devices, 1991, **ED-38**: 1432—1443.

[8] T. Ernst, S. Cristoloveanu, A. Vandooren *et al.*, Proceeding of 1998 IEEE International Conference, Oct., 1998, 21—22.

[9] A. S. Grove and D. J. Fitzgerald, S. S. E., 1966, **9**: 783—805.

[10] T. Giebel and K. Goser, IEEE Electron Device Lett., 1989, **10**: 76—78.

[11] Xue Jun Zhao and Dimitris E Ioannou, Proceeding of 1999 IEEE International SOI Conference, Oct., 1999, 52—53.

[12] T. Ernst, S. Cristoloveanu, A. Vandooren *et al.*, IEEE Trans. Electron Devices, 1999, **ED-46**: 1503—1509.

[13] B. J. Baliga, Modern Power Semiconductor Devices, New York, Wiley & Sons., 1995.

[14] User's Manual of DESSIS-ISE, 1998.

[15] D. K. Schroder, IEEE Trans. Electron Devices, 1997, **ED-44**: 160—170.