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A New Method for Optimizing Layout Parameter of an Integrated On-Chip Inductor in CMOS RF IC′s

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Abstract: Analyzing the influence on *Q* factor, which was caused by the parasitic effect in a CMOS RF on-chip integrated inductor, a concise method to increase the *Q* factor has been obtained when optimizing the layout parameter. Using this method, the *Q* factor of 7.9 can be achieved in a 5nH inductor (operating frequency is 2GHz) while the errors in inductance are less than 0.5% compared with the aimed values. It is proved by experiments that this method can guarantee the sufficient accuracy but require less computation time. Therefore, it is of great use for the design of the inductor in CMOS RF IC′s.

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1 Introduction

The deep sub-micrometer CMOS process, with which the transistor with a very high characteristic frequency (f_t) can be fabricated[1], enables the Si CMOS IC′s to be used widely in the frequency range of 900M—5GHz (radio frequency)[2]. Because Si is low in cost, mature in technology and easy to integrate, Si CMOS RF IC′s fabrication has the advantages over GaAs IC′s and the baseband circuit is of the frequency, which is lower than 2GHz[3]. But it is rather difficult to integrate an on-chip inductor with a factor (*Q*), that is high enough, on the bulk Si substrate during the fabrication of Si CMOS RF IC′s (such as VCO, LNA and the passive filter)[4]. Limitation in *Q* factor result from both the resistivity and small thickness of aluminum interconnects, and the losses in the conductive silicon substrate as well[5]. Recently, some researches on the integrated on-chip inductors are focused on how to improve the *Q* factor through the modification[6,7]. Should the standard process be changed, a series of problems will occur. For instance, the method of etching

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the substrate under the inductors can achieve a higher Q factor[6], but reduce the reliability, such as packaging yield and long-term mechanical stability. For the low cost integration of inductors, the increase in complexity of process should be avoided while we try to improve its performance. Without changing the standard process, optimizing the layout parameter to increase the inductor′s Q factor, therefore, will be of great value in the circuit design. In this paper, the parasitic effect of metal and substrate was analyzed at first. After studying the relationships between the Q factor and the layout parameter, we found that at a relative low frequency, the parasitic effect was mainly caused by the parasitic resistance, while at a relative high frequency, it was mainly caused by the parasitic capacitance. For this reason, the maximum ratio of the metal line′s width to its space is not the optimum one, as what the Reference[8] suggested. In order to obtain the highest Q at a special operation frequency (f_o), the ratio of the width to the space should be optimized. Because of the complication of computing the parasitic effect of the inductor, electromagnetic simulation, though generally applied in such computations, is very expensive, time consuming and hard to optimize. A method is proposed to determine the optimized layout parameter easily. Given the operation frequency f_o and the inductance of the inductor L, we can determine the optimum layout parameter at any frequency with great quickness and accuracy. Compared with the electromagnetic simulation, this method greatly reduces both the time and expense of the computation, and ensures the pinpoint accuracy in most operation frequency range. Using this method, the Q factor of 7.9 can be obtained in a 5nH inductor(operating frequency is 2GHz) and the errors in inductance is less than 0.5% compared with the aimed values. The final result of the experiment shows that the Q of the optimized inductor is very close to the calculated value, i.e. this method can be used effectively in the design of the inductor in CMOS RF IC′s.

2 Method of Optimization

The plan of the inductor is shown in Fig. 1, where n is the number of coils, w_i is the width of the metal lines, s is the space between the metal lines. The d_{in} and d_{out} is the inside and outside diameter of the inductor, respectively. The first step of optimization is to define the value of d_{in} and d_{out}. During the design, the layout parameter should be optimized subject to an unchanged special inductance. The n, w_i, s, d_{in} and d_{out} should be optimized for the highest Q under the qualtification of optimization, which is the relation between the inductance and the layout parameter. Greenhouse′s formula, the first way to calculate the inductance[9], is too complicated to be used in original design and optimizing. In this paper, an expression in Reference [10] is adopted.

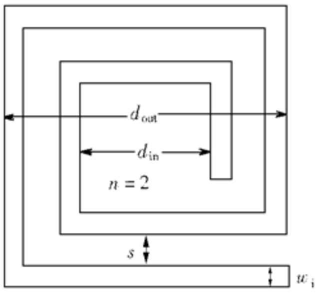

FIG. 1 Layout of On-Chip Inductor

$$L = K_1\mu_0 n^2 d_{avg}/(1 + K_2\rho) \tag{1}$$

$$\rho = (d_{out} - d_{in})/(d_{out} + d_{in}) \tag{2}$$

In the formula, K_1 and K_2 are both constants, and the d_{avg} is the average diameter.

$$d_{avg} = (d_{in} + d_{out})/2 \tag{3}$$

The essential conditions of optimization is simplified in this formula. Because there are still three layout parameters to be determined, namely n, d_{in} and d_{out}, we can take the following steps: first, suppose n is an integral number, all possible n could be considered in order to find the optimum one. According to the practical experience, for an inductor less than 10nH, n should range from 2 to 10. In addition, d_{out} will reach its possible maximum value when d_{in} equals to zero. As to a specific process, the minimum value of the space and that of the width are the minimum characteristic sizes. Accordingly, for 1μm process, we get:

$$d_{out} \geqslant d_{in} + 2[nw_i + (n - 1)g] = d_{in} + 2(2n - 1) \tag{4}$$

To a specific n, both the d_{in} and d_{out} that satisfy the inductance value can be found out. For the same n, as what the Reference[11] suggested, the larger the d_{in} is, the higher the Q will be. So, the combination of d_{in} and d_{out} can be used as the optimum under the condition that $d_{in} = \max(d_{in})$.

The second step is to determine the value of w_i and s. In the 1μm process, the minimum s equals to 1μm. Since the n, d_{in} and d_{out} have been determined, all values of w_i and s, which satisfy the expression (1), can be calculated. Being the integral multiple of the process characteristic size, w_i, s, d_{in} and d_{out} do not have the sequent values, which makes some errors of inductance in the inductor compared with aimed values.

The last step is to calculate the Q factor and determine the optimum layout parameter. The integrated on-chip inductor model is shown in Fig. 2. R in Fig. 2 is the series resistor of the metal line. C_{ox} is the parasitic capacitor between the second layer metal and the substrate. C_m is the parasitic capacitor between the two metals. C_{Si} is the parasitic capacitor of the substrate. R_{Si} is the resistor of the substrate. Values of these parasitic effects are:

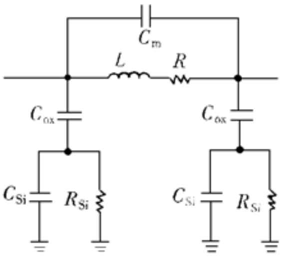

FIG. 2 Model of an Inductor

$$C_{Si} = \frac{w_i l \epsilon_{Si}}{2t_{Si}} \tag{5}$$

$$R_{Si} = \frac{t_{Si}}{2w_i l}\rho_{Si} \tag{6}$$

$$C_m = nw_i^2\frac{\epsilon_{ox}}{t_{ox}} \tag{7}$$

$$C_{ox} = \frac{w_i l \epsilon_{ox}}{2t_{ox}} \tag{8}$$

$$R = \frac{l}{w_i t}\rho_{Al} \tag{9}$$

The l is the total length of the metal line.

$$l = 4n[d_{\text{out}} - n(w_i + s)] \tag{10}$$

It is complicated to express the Q factor by a closed expression, so in this paper we directly calculate the reactance of each parasitic component, and then calculate the Q factor. When our connecting one port to the ground, all parasitic components (include R_{Si}, C_{ox}, C_{m} and C_{Si}) can be looked upon as one reactance Z_{P},

$$Z_{11} = Z_{\text{p}} \,/\!/\, Z_{\text{L}} \tag{11}$$

The reactance of the inductor itself is:

$$Z_{\text{L}} = R + j\omega L \tag{12}$$

The C_{Si} is in parallel connection with R_{Si} and they are in series with C_{ox}. Then all of these are in parallel with C_{m}, so the parasitic reactance is:

$$Z_{\text{p}} = [Z_{\text{ox}} + (Z_{\text{cSi}} \,/\!/\, Z_{\text{rSi}})] \,/\!/\, Z_{\text{m}} \tag{13}$$

The Q factor is:

$$Q = \text{imag}(Z_{11})/\text{real}(Z_{11}) \tag{14}$$

3 Design Example and Experiment Result

Now, we will explain the optimizing method through designing an inductor with a 5 nH inductance at 2GHz operation frequency.

The process is the 1μm CMOS technology with two metal (Al) layers. The thickness of the substrate is 500μm. The resistivity of the substrate is 15—20Ω• cm. The thickness of the first layer metal is 1μm. The thickness of the second layer metal is 2μm. The thickness of the oxide layer between the first layer metal and the substrate is 1μm. The thickness of the oxide layer between the second layer metal and the substrate is 3μm.

All the values of d_{in} and d_{out} that satisfy the inductance should be determined. Take $n = 4$ for example, from expression (2) and when $d_{\text{in}} = 0$, we can find that the maximum possible value of d_{out} is 797μm, meanwhile, d_{out} should satisfy the expression (3). For the sake of convenience, each d_{out} is a value between 1μm and 797μm, with 1μm´s adding per d_{out}. From all 797 d_{out}, all possible d_{in} can be determined by (2). The relationship between d_{in} and d_{out} is shown in Fig. 3 (the numbers are all of the possible combinations). The bigger the d_{in} is, the better the Q factor will be. So, the combination of d_{in} and d_{out} will be the optimum value when d_{in} is the maximum value. We can calculate all w_i and s values under this condition. The result of the calculation is listed in Table1. For the sake of convenience, the inductors are numbered by different w_i and s (note that this number differs from the number in Fig. 3). From Table 1, we can see that in order to satisfy the requirement that w_i and s

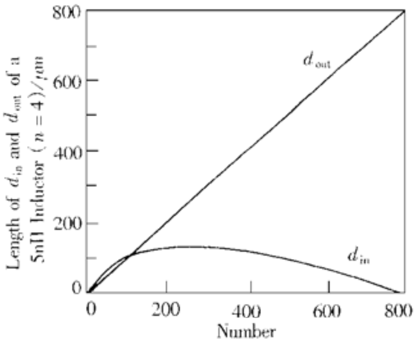

FIG. 3 Relationship Between d_{in} and d_{out}

Table 1 All of Width and Space of a 5nH Inductor with Max d_{in}(n= 4)

number	$d_{in}/\mu m$	$d_{out}/\mu m$	$w_i/\mu m$	$s/\mu m$	Errors/%
1	136	286	18	1	0.4
2	136	284	17	2	0.35
3	136	282	16	3	0.31
4	136	288	16	4	0.45
5	136	286	15	5	0.4
6	136	284	14	6	0.35
7	136	282	13	7	0.31
8	136	288	13	8	0.45
9	136	286	12	9	0.4
10	136	284	11	10	0.35
11	136	282	10	11	0.31
12	136	288	10	12	0.45
13	136	286	9	13	0.4
14	136	284	8	14	0.35
15	136	282	7	15	0.31
16	136	288	7	16	0.45
17	136	286	6	17	0.4
18	136	284	5	18	0.35
19	136	282	4	19	0.31
20	136	288	4	20	0.45
21	136	286	3	21	0.4
22	136	284	2	22	0.35
23	136	282	1	23	0.31

must be the integral multiple of 1μm, the value of d_{out} should be changed. This modification will bring some errors in the inductor inductance. All errors compared with the aimed values are less than 0.5%, as shown at the last row of the table. Anyway, this result is good enough for most of the circuit designs. From Table 1, it is found when the number of the inductors increases, the w_i/s decreases. Q factor, numbered 1, 5, 10 and 15 are shown in Fig. 4, as a function of frequency of inductor. In Fig. 4, at a big w_i/s, the higher Q factor can be obtained at a low frequency; on the other hand, when such a ratio decreases, the higher Q factor can be obtained at a high frequency. The frequency, at which the Q factor reaches its Q_{max}, will increase as the w_i/s decreases. When the frequency is 2GHz, number 5 inductor can get its optimum Q factor (Q_{max} = 7.9). The effect of w_i/s on the Q factor can be observed from the study of the parasitic effect. Figure 5 is the relationship between the parasitic parameter and the frequency of the inductor numbered 5 (w_i/s= 3). The imaginary part of Z_p can be regraded as the parasitic capacitance effect, while the real part of it as the parasitic resistance effect (as is conductance in the Fig. 5). It can be seen clearly from the Fig. 5 that when the frequency is low,

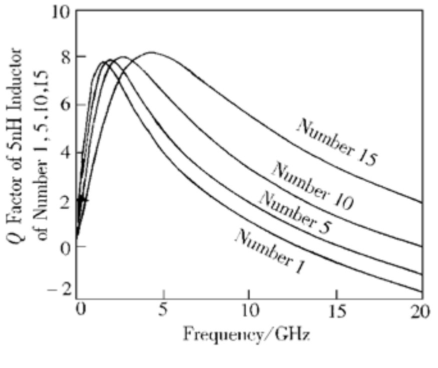

FIG. 4 Relationship Between Q Factor of Number 1, 5, 10, 15 and Frequency

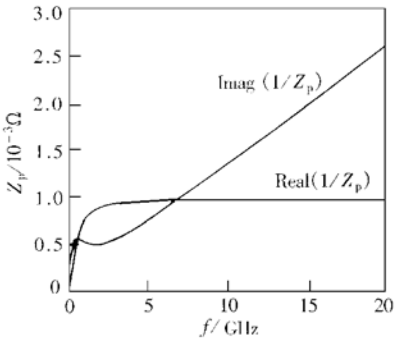

FIG. 5 Relationship Between Z_p and f

the parasitic capacitance effect is small while the parasitic resistance effect is on the contrary (when the conductance is small). While the frequency comes to a certain value, the parasitic resistance will become small and then keep constant when the frequency further increasing. On the other hand, the parasitic capacitance effect will enlarge with the increasing frequency and at last come to the a local maximum value at a certain frequency. The parasitic capacitance effect won´t decrease with the increasing frequency until it reaches a local minimum value at the frequency of about 2GHz.

Then it will go on increasing with the frequency, i. e. at the frequency of about 2GHz, both the parasitic resistance effect and the parasitic capacitance effect have the relatively small values, which makes the Q factor obtain its maximum value of 7.9. Because different ratio of w_i to s will alter the point of the frequency, at which the Q factor attains to it´s maximum value, the relationship between the w_i/s and each parasitic component can be analyzed. When w_i/s becomes large, the w_i will become large while the s small. From expression (9), it is known that l also becomes large. Thus, the capacitance that defined by expression (5), (7) and (8) will become large. Accordingly it is the C_{ox} that is the dominant parasitic capacitance during all of these capacitors. In addition, results from expression (6), (9) and (10) indicate that R and R_{si} will diminish. R is very important because of its series with the L. Figure 6 shows a relationship between the R, C_{ox} and the w_i/s. It is known that the parasitic resistor is the first cause to reduce the Q factor at a relatively low frequency, while the parasitic capacitor is the first cause at relatively high frequency. So if the application f_0 frequency is a low value to some extent, a big ratio of w_i/s would be selected. Otherwise, it would be better choice to select a small ratio. This conclusion is in accord with the proceeding discussion. After all, the optimum ratio of w_i/s is determined by the operation frequency according to the program of Matlab, the ultimate layout parameter is: $n = 4$, $w_i = 15\mu m$, $s = 5\mu m$, $d_{in} = 136\mu m$, $d_{out} = 286\mu m$. Using these layout parameters and the process aforementioned, an inductor integrated on-chip will be fabricated. All the measurements are taken with on-wafer RF probes and a HP8510C Network Analyzer. The comparison between experiment data and the theoretic ones is shown in Fig. 7, from which, it can be observed clearly that in the range of low frequency, two kinds of data are

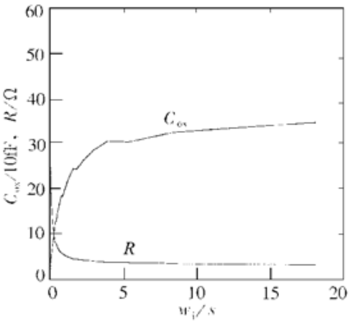

FIG. 6 Relationship Between R, C_{ox} and w_i/s

coincident well, with a good prediction of the Q factor. At the application frequency f_0 of 2GHz, the Q factor can obtain its maximum value of 7.9. When the frequency increases (to about 6 GHz or higher), there will exist some errors in the theoretic figure, because the model might be inaccurate in the high frequency considering the parasitic effect. Fortunately, most of RF CMOS IC′s are used in the frequency range of 900MHz to 5GHz, so this method is adequately accurate, with the outstanding advantages of time saving and low cost in computation.

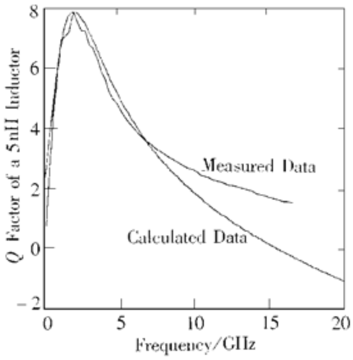

FIG. 7 Comparison Between Experiments Data and Theoretic ones

4 Conclusion

It is very important to optimize the layout parameter in the design of an integrated on-chip inductor in CMOS RF IC′s. In this paper, a new method of optimizing the layout parameter was proposed without using the electromagnetic simulation. Using this method, the Q factor of 7.9 is obtained at the operating frequency of 2GHz in a 5nH inductor, with some errors in the inductance less than 0.5% compared with the aimed values. Also, the ultimate layout parameters of a 5nH on-chip inductor are defined in this paper. Then the inductor was fabricated in a 1μm CMOS process. The comparison between the result of the experimental data and the calculated ones indicates that when the frequency is not very high, this method can ensure the accuracy of the computation but require less time and cost. So, this method can be used effectively to design the inductor in CMOS RF IC′s.

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