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An 8.5GHz 1∶8 Frequency Divider in 0.35 m CMOS Technology*

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Abstract: An 1∶8 frequency divider is designed and realized in a 0.35μm standard CMOS technology. The chip consists of three stages of 1∶2 divider cells, which are constructed with source couple logic (SCL) flip-flops. By revising the traditional topology of SCL flip-flop, a divider with better performances is got. The results of measurement show that the whole chip achieves the frequency division at more than 8.5GHz. Each 1∶2 divider consumes about 11mW from a 3.3V supply. The divider can be used in RF and optic-fiber transceivers and other high-speed systems.

Key words: frequency divider; flip-flop; CMOS; IC
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1 Introduction

Flip-flop based on high-speed frequency dividers are often used as showcases for high-speed technologies. In Si/SiGe bipolar or Ⅲ/Ⅴ compound technologies, such as GaAs and InP, frequency divider can easily achieve an operation frequency over 50GHz[1,2]. However, as the feature size of CMOS technology is getting smaller in recent years, the cut-off frequency of CMOS technology is getting much higher[3], revealing the potential of CMOS technology for high-speed applications. In fact, there are some CMOS dividers with new topologies achieving a very high speed[4~6].

For dividers in practical systems, there are some essential requirements. The first is good interface with other circuits in the same system, that is, the DC off-sets, signal swing, and I/O impendent of the divider should match its former and latter circuits. The second is strong stability, which means the divider should resist all kinds of interferences, such as variation of supply voltage. The third is wide range of operation, that means the divider can work rightly in a large range of frequency. The forth is high sensitivity to swing of input signal. Other requirements are low power, small die area, etc., which are necessary requirement for most function circuits.

To get a divider meet these requirements, SCL (source coupled logic) topology is a good choice. Similar with SCFL (source coupled FET logic) in GaAs circuit family and ECL (emitter coupled logic) in Si bipolar circuit family, SCL is a valuable logic type of CMOS technology[7].

This paper presents SCL 8.5GHz frequency divider in 0.35μm standard CMOS technology. By revising the traditional topology of SCL flip-flop, we got a divider with better performances. The results of measurement show that the whole chip

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achieves the frequency division at more than 8.5GHz. Part 2 shows the details of the circuits. The manufacturing aspects and measuring results are given in parts 3 and 4.

2 Circuits design aspects

Figure 1 shows the block diagram of the whole chip. The 1∶8 divider is built up with three stages of SCL 1∶2 frequency dividers. The first stage is a dynamic frequency divider, and it determines the performance of the whole chip. The second and third stages are two identical static dividers, which can work stably at low frequency. 50Ω input matching resistors and output buffers are designed on chip for the purpose of testing.

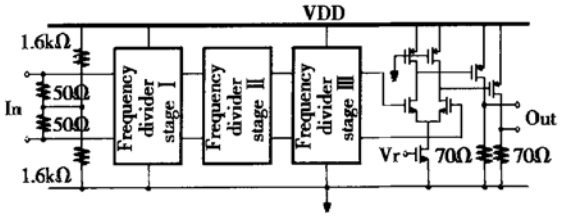

Fig. 1 Block diagram of the 1∶8 frequency divider IC

The circuit topology of the first stage is the same as the other two, but the configurations of their transistors are different. As shown in Fig. 2, the SCL 1∶2 divider is based on the high-speed latching flip-flop (HLO-FF)[8]. The main difference between HLO-FF and master slave delay flip-flop (MSDFF) is that: in an HLO-FF, the series-gate connection separates the current paths of the reading and latching circuits, while in an MSDFF, in both the master and slave latches, current switches of reading and latching pairs share the same current path. That is, in Fig. 2, MRS1 of the master latch and MRS2 of the slave latch, which are current switching pair of reading circuits, share the tail current source, MCSR; while MLS1 of the master latch and MLS2 of the slave latch, which are current switching pair of latching circuits, share the tail current source, MCSL. This topology brings forth important advantages: (1) all current pairs of both reading and latching circuits contain two symmetric MOSFETs, thus keeping all the merits of symmetric differential circuits; (2) the ratio between the currents of reading and latching circuits can be easily set by adjusting the transistor size ratio of MCSR and MCSL; (3) comparing with the MSDFF topology, higher speed can be achieved by the frequency divider based on this topology due to its shorter delay time[6].

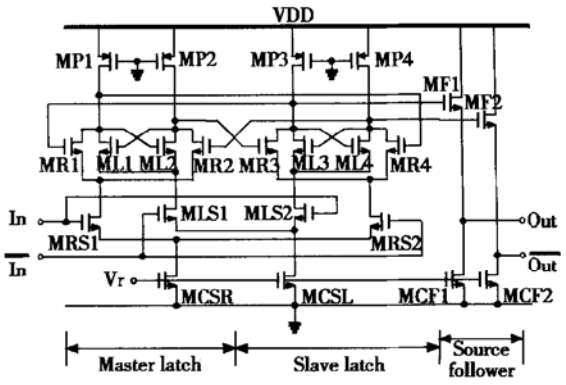

Fig. 2 Schematic of the SCL 1∶2 frequency divider

At ultra-high-speeds, the resistance of the loads in an SCL circuit should be very accurate. But CMOS passive resistors, usually made of poly silicon, suffer a process variation as large as ±20%. That is the reason we use PMOSFETs as loads, instead of passive resistors. The gates of the PMOSFET are grounded so that the devices work in the linear region, serving as loads with relatively constant resistance.

By setting the voltage level appropriately, source followers (SF), commonly used in GaAs SCFL circuits for level shifting between master and slave latches, are omitted here. This helps improve the speed of the divider. However, two SFs are still needed after the slave latch to make the level of the output suitable to next stage.

3 Manufacturing aspects

The frequency divider IC is designed and realized in a 0.35μm double-poly four-metal N-well

standard CMOS technology through MOSIS. Simulations show that this CMOS process has a cut-off frequency (f_T) about 13.5GHz. The die photograph of the frequency divider is shown in Fig. 3. The size of the chip is about 0.5mm×0.44mm. Every 1∶2 frequency divider cell is only about 35μm ×50μm.

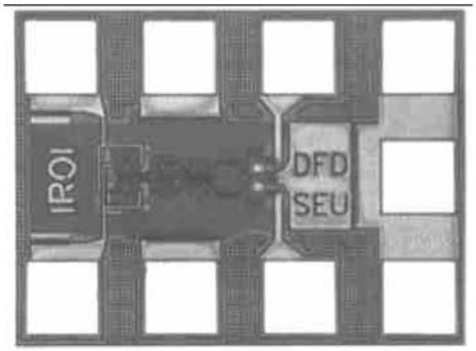

Fig. 3 Die photography of the frequency divider IC

4 Experimental results

The chip is mounted on a ceramic substrate, which is soldered on a brass block. Pads of the chip are connected with microstrip lines on the ceramic substrate by bonding wires. In this way, we tested the chip without a probe station.

The chip is tested with a 3.3V supply. The differential input clock signal is fed into the chip via Bias-Tees. Measured minimum input voltages (required at each end of the differential inputs to sustain the operation) at different input frequencies are shown in Fig. 4, which also shows the bandwidth of the divider is about 2GHz under the condition that the input swing is not larger than 0.8V. Larger input swing can get higher operation frequency and wider bandwidth. Figure 5 shows the measured input and output waveforms when the input is 8.5GHz with a swing of 0.8V.

The DC power dissipation of the whole chip is about 90mW. According to simulation results, each stage of the two 1∶2 dividers consumes about 12% of the whole power dissipation, that is, about 11mW in reality.

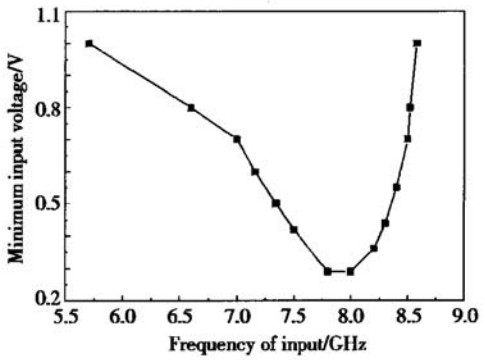

Fig. 4 Measured minimum input voltage vs input frequency

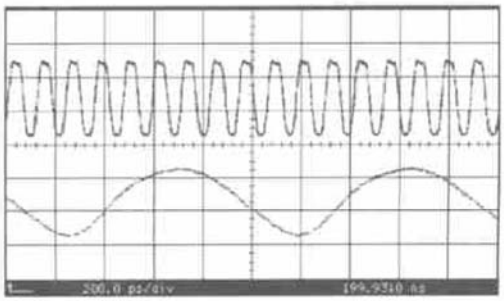

Fig. 5 Measured waveforms with an 8.5GHz input

5 Conclusion

An SCL 1∶8 frequency divider has been realized with a 0.35μm standard CMOS technology. Under a 3.3V supply, this divider can work at more than 8.5GHz. Each 1∶2 divider cell consumes a power dissipation of 11mW and has a size of 35μm×50μm. The divider can be used in high-speed RF and optic-fiber transceivers. These results not only proved the value of the SCL logic style but also demonstrated the potential of 0.35μm CMOS as a technology for high-speed applications.

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0.35 m CMOS 8.5GHz 1∶8 分频器的设计*

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摘要: 实现了一个基于触发器结构用 0.35μm CMOS 工艺实现的 1∶8 分频器. 它由 3 级 1∶2 分频器单元组成, 其中第一级为动态分频器, 决定了整个芯片的性能, 第二、三级为静态分频器, 在低频下能稳定工作. 分频器采用源极耦合逻辑电路, 并在传统的电路结构上进行改进, 提高了电路的性能. 测试的结果表明, 芯片工作速率超过 8.5GHz, 工作带宽大于 2GHz. 电路在 3.3V 电源电压下工作, 每个 1∶2 分频器单元的功耗约为 11mW, 面积为 35μm×50μm. 该芯片可应用于高速射频或光电收发机系统中.

关键词: 分频器; 触发器; CMOS; 集成电路

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