

# Minority-Carrier Exclusion Effect in Thin-Film SOI Temperature Sensor\*

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**Abstract:** A silicon temperature sensor with a conventional resistor structure is fabricated on thin-film silicon-on-insulator (SOI) substrate. The sensor has very promising characteristics. The maximum operating temperature can reach 550°C even at a low current of 0.1 mA. Experimental results support that the minority-carrier exclusion effect can be strong in the conventional resistor structure when the silicon film is sufficiently thin, thus significantly raising the maximum operating temperature. Moreover, since the structure of the device on thin-film SOI wafer is not crucial in controlling the maximum operating temperature, device layout can be varied according to the requirements of applications.

**Key words:** minority-carrier exclusion effect; high temperature sensors; spreading resistance; SOI

**PACC:** 7200; 7220; 7360

**CLC number:** TN379

**Document code:** A

**Article ID:** 0253-4177(2003)05-0461-05

## 1 Introduction

Currently, there is a strong demand for electronic devices that can operate over wide temperature range. This is required for electronics used in the high-temperature portions of cars and aircrafts. Moreover, this demand is further increased by the development of high fidelity sensors and control circuits used in space rockets, nuclear reactors, and geothermal power generators. High-temperature sensors based on wide band-gap semiconductors such as SiC have also been investigated in attempts to produce electronic devices operating reliably even at high temperatures. However, devel-

oping wide band-gap semiconductors into sensors is so difficult that it will take a long time for them to become practical devices. Therefore, the development of high-temperature sensors based on commonly used silicon and related technologies still continues.

It is well known that the maximum operating temperature of conventional silicon sensors is limited to about 200°C, due to excessive thermal generation of carriers at higher temperatures. By utilizing the minority-carrier exclusion effect, the spreading-resistance temperature (SRT) sensor is proposed and the maximum operating temperature can be as high as 350°C<sup>[1]</sup>. One of the recent improvements on the SRT sensor is the use of a lateral struc-

\* Project supported by the University of Hong Kong CRCG and Hong Kong RGC (No. HKU 7045/98E)

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ture<sup>[2,3]</sup>, which gives a possibility to integrate the device with other circuits on a chip. This lateral SRT sensor needs a special structure to enhance the minority-carrier exclusion effect and hence to raise the maximum operating temperature. Moreover, SRT sensor fabricated on a silicon island of SOI wafer<sup>[4]</sup> has been demonstrated to be a promising structure, with preliminary results indicating that the exclusion effect can be enhanced for SRT device made on thin silicon film. However, so far, only in special asymmetrical structures (e. g. SRT structure), the minority-carrier exclusion effect is strong enough to raise  $T_{max}$ . Based on extensive study on the minority-carrier exclusion effect<sup>[5-11]</sup>, it is hoped that even for symmetrical structures, the silicon-film thickness in SOI substrate can provide another dimension for improving the positive-temperature-coefficient characteristics of the sensor resistance through the confinement of current flow in the thin silicon film. Thus, in this paper, a diffused resistor with the conventional structure is made on thin-film ( $1.2\mu\text{m}$ ) SOI, as depicted in Fig. 1. Experimental results show that a pronounced exclusion effect happens in the device and the maximum operating temperature can exceed  $550^\circ\text{C}$  even when the device operates at a low current of  $0.1\text{mA}$ . Furthermore, preliminary results reveal that the structure of the device on a thin-film SOI wafer is not so important in extending the maximum operating temperature, and therefore, device layout is flexible and applications can cover a much wider area.

## 2 Device fabrication

Figure 1 shows the structure of a conventional diffused resistor on SOI substrate with the two  $1.2\mu\text{m}$   $n^+$  regions stopped at the buried oxide. The wafer was formed by separation-by-implantation-of-oxygen (SIMOX) technique with an  $n$ -type  $\langle 100 \rangle$  silicon-film thickness of  $1.2\mu\text{m}$ , and a buried-oxide thickness of  $0.4\mu\text{m}$ . The silicon film had a resistivity of  $0.05 \sim 0.1\Omega \cdot \text{cm}$ . After oxida-

tion and  $n^+$  diffusion, a double layer of Ti-W ( $100\text{nm}$ )/Au( $300\text{nm}$ ) was sputtered as electrodes which can ensure stable operation even at high temperatures. Finally, post-metallization annealing was done at  $600^\circ\text{C}$  for 20min in  $\text{N}_2$  to make good contacts to the sensors. Dices of the wafer were attached to metal holders by standard glue. All wire bondings were done using gold wires. Electrical contacts to the pins of the packages were realized by wire wrapping using Teflon-coated electrical wire. The sensors were characterized between room temperature and  $550^\circ\text{C}$  under constant-current condition. The measurements were performed in a computer-controlled oven. Bias currents ranged from  $0.1\text{mA}$  to  $2\text{mA}$ .

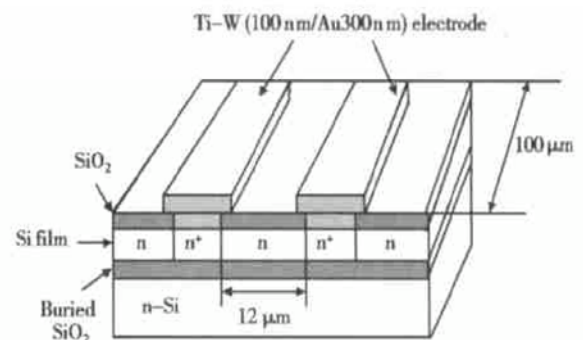


Fig. 1 Structure of SOI conventional resistor with  $L = 12\mu\text{m}$  and  $W = 100\mu\text{m}$

## 3 Results and discussion

The device resistance versus temperature at different current levels for the thin film SOI resistor is shown in Fig. 2, from which the maximum operating temperature of the device can exceed  $550^\circ\text{C}$ . The results imply that the minority-carrier exclusion effect happens in the conventional resistor structure on the thin silicon film, and hence significantly raises the maximum operating temperature.

The minority-carrier exclusion effect is one of the four semiconductor transport effects (minority-carrier injection, exclusion, accumulation, and extraction), which can occur at a semiconductor junction<sup>[12]</sup>. Exclusion of minority carriers is a (current

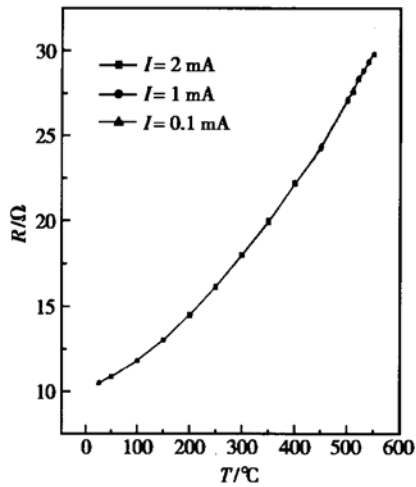


Fig. 2 Temperature dependence of the resistance of thin-film SOI conventional resistor ( $L = 12\mu\text{m}$ ) at different current

dependent) local minority carrier deficiency near a junction at a semiconductor boundary which injects less minority carriers into the semiconductor than that required for undisturbed bulk conduction, so that the bulk electric field removes minority carriers from the junction region faster than the junction supplies them, creating the deficiency. This semiconductor transport effect results in a drastic reduction in concentration of thermally generated carriers and thus maintains extrinsic carrier concentration even at high temperatures. This becomes the basic working principle of high-temperature silicon sensor. The extent of exclusion depends strongly on the electric field/current density in the bulk; higher field/current extracts more minority carriers. At sufficiently high current densities, excessive amount of thermally generated minority carriers can be almost completely removed, restoring the extrinsic carrier concentration. The mathematical analysis of the exclusion phenomenon in intrinsic silicon is very complicated, and different simplifications and numerical solutions have been proposed<sup>[5-11]</sup>. In the case of one-dimensional  $n^+n$  junction, remarkable minority-carrier exclusion happens under a current density of  $100\text{A}/\text{cm}^2$  at  $400^\circ\text{C}$ <sup>[13]</sup>. In two-dimensional or three-dimensional minority-carrier transport, the injection of minority

carriers into the exclusion region should be considered, so that minority-carrier exclusion in bulk-Si devices can be observed only for special asymmetrical structures such as a single point contact on an infinite slab of silicon<sup>[1-3,12,13]</sup>. In thin-film SOI devices, minority-carrier flow is limited to a very narrow region and a quasi one-dimensional transport is achieved. Even in the case of conventional resistor structure shown in Fig. 1, a small bias current of  $0.1\text{mA}$  gives a current density of about  $100\text{A}/\text{cm}^2$ , which is sufficiently high to extend the maximum operating temperature of the device. It is interesting that the results for bias currents of  $1\text{mA}$  and  $2\text{mA}$  are almost identical to that of  $0.1\text{mA}$ , probably because minority carriers are almost exhausted within the  $12\mu\text{m}$  wide region between the two electrodes of the device for bias currents as low as  $0.1\text{mA}$ . To verify this, Figure 3 shows the calculated minority-carrier concentration  $p$  in the  $n$  region

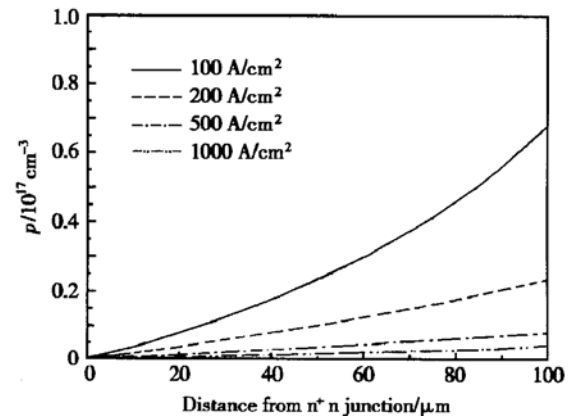


Fig. 3 Calculated minority-carrier concentration  $p$  for high-level exclusion in an  $n$ -type silicon region at  $550^\circ\text{C}$   $N_d = 10^{17}\text{cm}^{-3}$ ,  $b = \mu_n/\mu_p = 3$ , excess-carrier lifetime  $\tau = 10\mu\text{s}$

of an  $n^+n$  diode at  $550^\circ\text{C}$  for different current densities  $J$ , according to<sup>[13]</sup>

$$p = \frac{qbGN_{dx}}{J - q(b+1)Gx} \quad (1)$$

where  $b$  represents the ratio of electron and hole mobilities,  $N_d$  represents the doping level of the  $n$  region,  $x$  represents the distance from the  $n^+n$  junction in the  $n$  region. The generation rate of carrier is given by

$$G = \frac{1}{\tau} \times \frac{n_i^2}{N_d + 2n_i} \quad (2)$$

where  $n_i$  is the intrinsic carrier concentration and  $\tau$  is the excess-carrier lifetime. For all the devices in this work,  $N_d$  measured by spreading-resistance method equals to  $10^{17} \text{ cm}^{-3}$ . It is seen that for a  $12 \mu\text{m}$  wide region, the carrier concentration  $p$  is effectively reduced to extrinsic levels even at the lowest current density of  $100 \text{ A/cm}^2$ , because  $p$  at  $x = 12 \mu\text{m}$  is calculated to be only  $0.03N_d$ , which means that the device still has a very large exclusion region at  $550^\circ\text{C}$ . Therefore, the maximum operating temperature can be greatly raised to as high as  $550^\circ\text{C}$ . For the sake of comparison, resistors with longer lengths ( $500 \mu\text{m}$  and  $1000 \mu\text{m}$ ) are also characterized at a low current of  $0.1 \text{ mA}$ . Their results are shown in Fig. 4 and Fig. 5, with maximum operating temperatures of  $410^\circ\text{C}$  and  $350^\circ\text{C}$  respectively, illustrating that the exclusion effect can extend to a pretty wide region. All these observations demonstrate again that thin-film SOI can provide an extra dimension for improving the characteristics of the sensors.

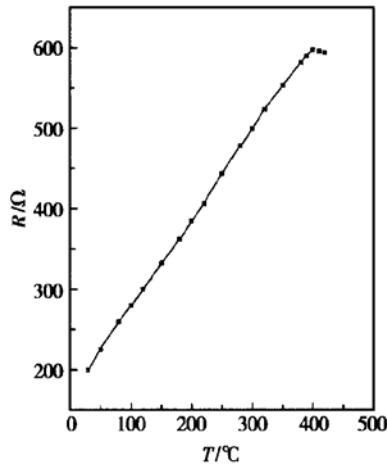


Fig. 4 Temperature dependence of the resistance of thin-film SOI conventional resistor with  $L = 500 \mu\text{m}$  at a low current of  $0.1 \text{ mA}$

## 4 Conclusion

A silicon temperature sensor with a conventional resistor structure is fabricated on thin-film

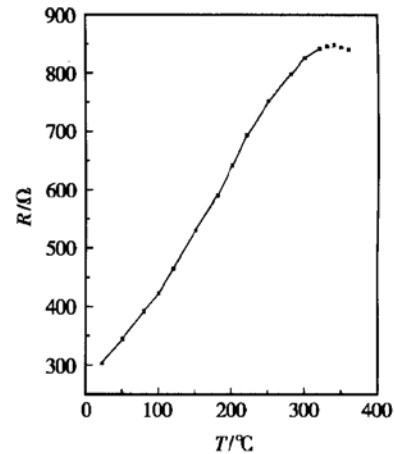


Fig. 5 Temperature dependence of the resistance of thin-film SOI conventional resistor with  $L = 1000 \mu\text{m}$  at a low current of  $0.1 \text{ mA}$

silicon-on-insulator substrate. The sensor has promising characteristics. Its maximum operating temperature can reach as high as  $550^\circ\text{C}$ . Experimental results support that the minority-carrier exclusion effect becomes significant in the conventional resistor structure when the silicon film is sufficiently thin, and hence greatly extends the operating temperature range of the device. Furthermore, since the structure of the device on thin-film SOI is not a dominant factor, the device can have a more flexible layout, thus covering a wider of scope of applications.

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## 薄膜 SOI 温度传感器中的少数载流子排斥效应\*

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**摘要:** 在薄膜 SOI 衬底上制备普通电阻结构的硅温度传感器, 并具有令人满意的特性: 即使在 0.1mA 的低偏置电流下, 器件的最高温度工作温度仍能达到 550°C. 实验结果分析说明, 当硅膜足够薄时, 普通电阻结构中可表现出较强的少数载流子排斥效应, 大大提高了本征转折温度, 从而提高器件的最高工作温度. 同时, 由于薄膜 SOI 温度电阻的结构对器件最高工作温度的影响不大, 因而传感器的器件结构可以根据需要来选择.

**关键词:** 少数载流子排斥效应; 高温传感器; 扩展电阻; SOI

**PACC:** 7200; 7220; 7360

**中图分类号:** TN379

**文献标识码:** A

**文章编号:** 0253-4177(2003)05-0461-05

\* 香港大学 CRCG 和香港 RGC(No. HKU7045/98E) 资助项目

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2002-10-11 收到, 2002-12-13 定稿