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Heteroepitaxial Growth and Heterojunction Characteristics of Voids-Free n-3C-SiC on p-Si(100) *

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Abstract: Highly oriented voids-free 3C-SiC heteroepitaxial layers are grown on φ50mm Si (100) substrates by low pressure chemical vapor deposition (LPCVD). The initial stage of carbonization and the surface morphology of carbonization layers of Si (100) are studied using reflection high energy electron diffraction (RHEED) and scanning electron microscopy (SEM). It is shown that the optimized carbonization temperature for the growth of voids-free 3C-SiC on Si (100) substrates is 1100℃. The electrical properties of SiC layers are characterized using Van der Pauw method. The *I-V*, *C-V*, and the temperature dependence of *I-V* characteristics in n-3C-SiC/p-Si heterojunctions with AuGeNi and Al electrical pads are investigated. It is shown that the maximum reverse breakdown voltage of the n-3C-SiC/p-Si heteroiunction diodes reaches to 220V at room temperature. These results indicate that the SiC/Si heterojunction diode can be used to fabricate the wide bandgap emitter SiC/Si heterojunction bipolar transistors (HBT's).

Key words: LPCVD; voids-free n-3C-SiC/p-Si(100); heterojunction characteristics
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1 Introduction

SiC has over 250 different one-dimensional polytypes. However, there is only one repetitive ABC stacking sequence yielding a zincblende structure, referred to as 3C-SiC or β-SiC. 3C-SiC has a wide bandgap of 2.2eV, a theoretical electron saturation drift velocity of 2×10^7cm/s, a high breakdown field of 5×10^6V/cm, and a high thermal conductivity of 3.5W/(cm · K). These properties make it important for potential applications in high-power-density, high-temperature, and high-frequency electronic devices as well as devices operating in a harsh environment[1]. The combination of SiC films with the well-known Si technology holds the promise for opening up new electronic applications. On the other hand, the epitaxial growth of SiC on Si substrates is of advantage because of the considerable lower costs, larger wafers and, 3C-SiC on Si could be used for the fabrication of heterojunction diodes (HJDs), heterojunction bipolar transistors (HBTs), junction field effect transistors (JFETs), metal semiconductor field-effect transistors (MESFETs), and robust sensors[2-5].

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Chemical vapor deposition (CVD) is presently the most widely used epitaxial technique for growth of SiC active structure at atmospheric or reduced pressure and at temperatures ranging from 1300℃ to 1360℃[6,7]. However, voids in the shape of inverted pyramids are often formed in Si substrate surfaces during growth of SiC by Si out-diffusion at high temperature, which significantly affects the electrical properties of SiC/Si heterojunctions[8,9]. Previously we reported the growth of 3C-SiC films grown on Si and sapphire complex substrates using MBE and/or LPCVD in a modified MBE system and an improved epitaxial growth of single crystalline 3C-SiC layers on Si (100) substrates by a rectangular shaped stainless steel CVD/LPCVD system at 2.67×10^4Pa[10~13]. In this paper, we report the LPCVD growth and electrical properties of voids-free n-3C-SiC/p-Si and heterojunction characteristics in a high vacuum system.

2 Experiment

The heteroepitaxial growth of SiC on Si (100) substrate has been performed by LPCVD in a modified MBE system at a pressure of 2.67×10^4Pa. The substrates used for 3C-SiC growth were φ50mm p-type Si (100) wafers with resistivity of 10~ 12Ω·cm. The Si (100) substrates were subjected to a pre-growth etching in hydrogen at about 1200℃ for 10min to remove any trace of contamination and to produce a surface suitable for carbonization and subsequent epitaxy. In this work, SiH_4, C_2H_4, and Pd-cell purified H_2 were used as precursor gases. The flow rates of SiH_4, C_2H_4, and H_2 were 0.5, 0.5, and 3000sccm, respectively. In order to prevent the formation of voids and to obtain improved interface of 3C-SiC/Si, much attention has been paid to the pretreatment and carbonization process of the substrates.

The surface morphology of the carbonization layers was investigated using scanning electron microscope (SEM) and reflection high energy electron diffraction (RHEED). The electrical properties of the epilayers were characterized using Hall effect measurements in the temperature range from 80 to 300 K. The magnetic field was 0.2T. Thickness of the epitaxial layers was determined by cleaving the sample and then examing them under a Nomarski optical microscope and/or SEM.

The heterojunction diodes with about 1mm×1mm in area were obtained by cleaving n-3C-SiC/p-Si along [110] direction. The typical sample parameters of 3C-SiC epilayers and Si substrates used to fabricate HJDs in this work are shown in Table 1. Al and AuGeNi were used to create ohmic contacts on Si and 3C-SiC by using evaporation followed by annealing at 750℃ and 650℃ for 10min, respectively. The specific ohmic contact resistivity of AuGeNi to n-type 3C-SiC of 1.12×10^{-5}Ω·cm was measured and obtained by linear transmission line method (L-TLM). The I-V and C-V characteristics were obtained using H-P 4140B and H-P 4284A, respectively.

Table 1 Parameters of 3C-SiC epilayer and Si substrate

Properties	3C-SiC	Si
Energy bandgap/eV	2.2	1.1
Resistivity/(Ω·cm)	0.01~ 0.03	10~ 12
Conduction type	n	p
Carrier concertration/cm^{-3}	$(7\sim 12)\times10^{17}$	2×10^{15}
Mobility/($cm^2\cdot V^{-1}\cdot s^{-1}$)	460~ 490	340
Sample thickness/μm	1~ 2	380
Dielectric constant	9.7	11.9

3 Results and discussion

Due to the large lattice mismatch (20%) between Si and 3C-SiC, a buffer (or carbonization) layer is necessary for the subsequent growth of a crystalline SiC film. Buffer layer formation is influenced by preparation conditions. In order to obtain the optimum carbonization conditions, the carbonization processes by LPCVD at different temperature, carbonization time, and growth pressure were investigated. Figure 1 shows the RHEED patterns observed before and after carbonization of Si (100) at 1200℃ and at 1100℃ for 10min. The cor-

responding SEM plane view micrographs are shown on the right. The incident electron beam is parallel to the 〈110〉 direction. Figure 1(a) shows a clean and smooth Si (100) surface obtained before carbonization. If the carbonization temperature is higher than 1200℃, the RHEED pattern of the carbonized layer contained faint rings, indicating a polycrystalline carbonized layer as shown in Fig. 1 (b). It can be seen from the corresponding SEM image that voids appearing dark were formed during carbonization at 1200℃, which indicates the out-diffusion of Si atoms from the substrates. However, the carbonization surface at 1100℃ was featureless and mirror-like indicating no obvious Si out-diffusion occurred. It is evident from Fig. 1(c) that a single crystalline 3C-SiC carbonized layer without any twin spots was obtained at 1100℃. This is the optimized carbonization temperature used in this work. Using this technique, the optimized carbonization time of 10min and growth pressure of 2.67×10^4Pa were obtained for this growth system. The best full width at half maximum (FWHM) of about 0.5° of a double-crystal X-ray rocking curves for SiC (100) at $2\theta = 41.4°$ of the final LPCVD 3C-SiC epitaxial layers was examined and obtained under this optimized condition.

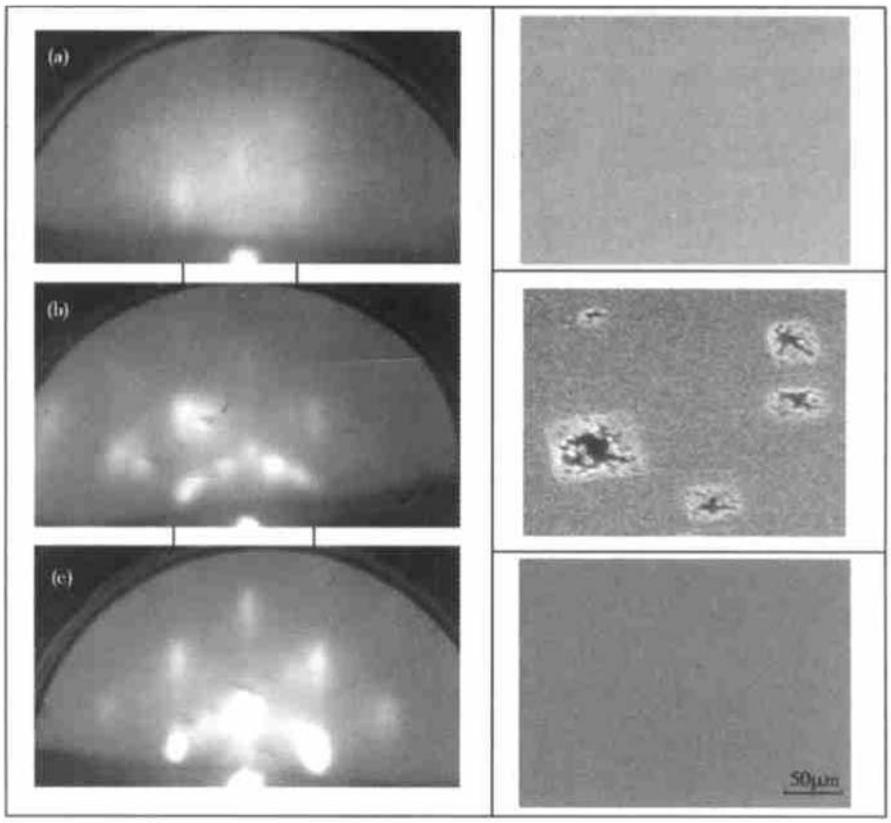

Fig. 1　RHEED patterns observed before (a) and after carbonization of Si(100) at 1200℃ (b) and at 1100℃ (c). The corresponding SEM plane view micrographs are shown on the right.

Figure 2 shows six cross-sectional SEM images at different position along the diameter of a φ50mm 3C-SiC/Si sample cleaved along 〈110〉 direction. This sample was grown at 1200℃ for 2h. Even the growth temperature is higher than that for carbonization, it can be seen that there is no obvious voids (typical size in micron) formed in the Si substrate surface. This result indicates that the voids were mainly formed during carbonization process and the out-diffusion of Si atoms from Si substrates was suppressed by the carbonization layer during the epitaxial growth of SiC at higher

temperatures. It can also be obtained that the thickness uniformity determined by SEM is better than 95%.

Hall effect measurements were performed to investigate the electrical properties of the grown 3C-SiC films using Van der Pauw method. Figure 3 shows the temperature dependence of free electron concentration and Hall mobility in the temperature range from 80 to 300K. The temperature behavior is similar to what obtained in Ref. [12]. The carrier concentration was about $3.0\times10^{16}\,cm^{-3}$ at room temperature. The room temperature Hall mobility was $690cm^2/(V\cdot s)$ and the highest mobility reaches $1510cm^2/(V\cdot s)$ at 150K.

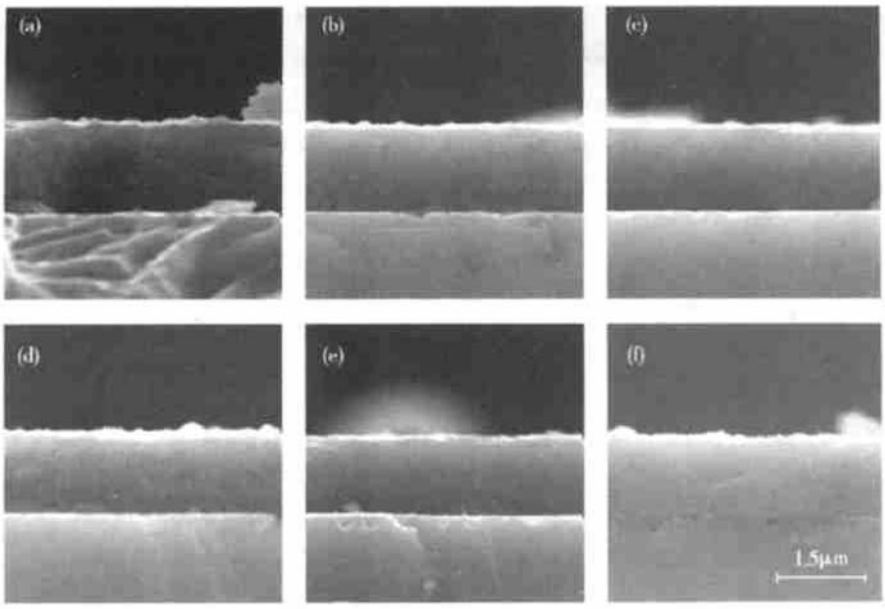

Fig. 2 Six cross-sectional SEM images at different position along the diameter of a φ50mm 3C-SiC/Si sample cleaved along 〈110〉 direction

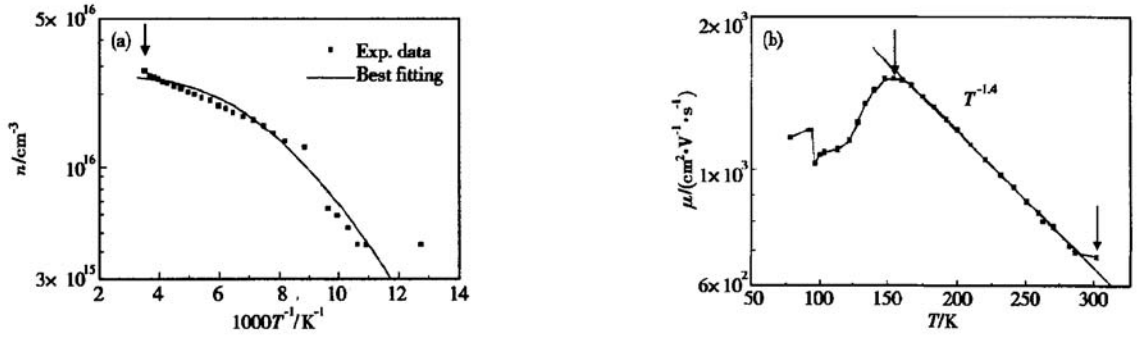

Fig. 3 Temperature dependence of free electron concentration (a) and Hall mobility (b) The solid line in (a) is the best fittings result using equation (1) and the solid in (b) shows the $T^{-\alpha}$ rule, where $\alpha=1.4$.

From above results, unintentionally doped 3C-SiC layers show n-type conduction. The origin of this n-type conduction is controlled by a shallow donor of nitrogen (N)[14]. It is well known that nitrogen is also commonly used as the n-type dopant in 3C-SiC. Ionization energy ΔE and concentration N_D of the prevailing dopant N, as well as the concentration of the compensation N_{comp}, can be obtained from a fit of the neutrality equation (1) to the temperature variation of the measured free

electron carrier concentration (n)[15].

$$n + N_{comp} = \frac{N_D}{(gnN_C(T))\exp(\Delta E/kT) + 1} \quad (1)$$

where $g = 2$ is the spin degeneracy factor, $N_C(T)$ is the density of states in the conduction band and can be described by the following equation (2)[13]

$$N_C(T) = 3.0 \times 10^{15} T^{3/2} \quad (2)$$

From the Hall analysis, we obtained $\Delta E = 49$meV, $N_D = 2.7 \times 10^{16}\,cm^{-3}$, $N_{comp} = 7.0 \times 10^{15}\,cm^{-3}$. The ionization energy is close to the published values obtained by Hall measurements[17], donor-acceptor pair photoluminescence[14], and effective mass approximation[16].

Figure 4 shows the I-V and C-V characteristics of the 3C-SiC/Si heterojunction diodes with about 1mm × 1mm in area. It was shown in Fig. 4 (a) that at low current densities the dependence of the forward current on voltage is exponential $J = J_0\exp(qV/\eta kT)$ with the ideality factor of η which is about 1.62 at room temperature. The maximum

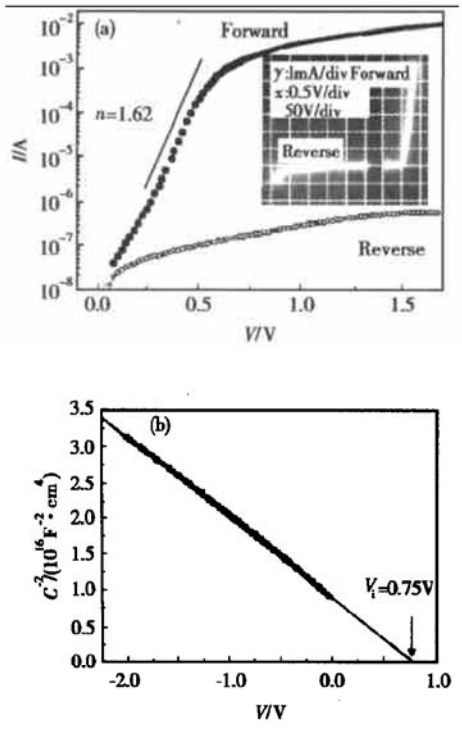

Fig. 4　I-V (a) and C-V (b) characteristics of n-3C-SiC/p-Si HJDs

reverse breakdown voltage reaches 220V. The current rectification ratio defined at ±1V bias reaches to 1.5×10^4. The effect of temperature on the J-V characteristics of the SiC/Si HJD was also investigated. Over the temperature range of 20 to 100℃, the current rectification ratio is observed to decrease with temperature from 1.5×10^4 to 86. Slightly rectifying characteristics were also observed at an ambient temperature of over 200℃. The C-V characteristics of the diode were linear in the C^{-2}-V coordinates as shown in Fig. 4(b), which means that the obtained n-3C-SiC/p-Si heterojunctions were abrupt. A built-in voltage (V_{bi}) of 0.75V was obtained by extrapolation of the linear dependence to $C^{-2} = 0$.

At room temperature, the energy band gap of 3C-SiC and Si is 2.2eV[10] and 1.1eV, respectively. When 3C-SiC is epitaxially grown on Si substrate, a 3C-SiC/Si heterojunction is formed. A built-in electric field is produced from the n-SiC to the p-Si across the interface. It has been shown from the C-V result that the p-n heterojunction is abrupt. Thus the depletion widths were obtained by solving Poisson's equation for the step junction on either side of the interface. According to the typical data of n-3C-SiC and p-Si given in Table 1 and the value of obtained built-in potential, the depletion widths in the Si side is 0.7μm and that of in the SiC side is 1.2nm. These results indicate that most of the depletion region is in the Si side. Therefore, the interface quality between 3C-SiC and Si substrate is important, especially the surface quality of Si substrate. It can be concluded that a smooth surface of carbonization layer, i. e. the suppression of voids in Si surface is critical to improve the quality of 3C-SiC/Si heterojunctions.

4　Conclusion

In a CVD/MBE high vacuum system, highly oriented voids-free 3C-SiC heteroepitaxial layers have been grown on φ50mm Si (100) substrates by LPCVD. The initial stage of carbonization and the surface morphology of carbonization layers of Si (100) have been studied using RHEED and SEM.

It has been shown that the optimized carbonization temperature is 1100℃ for Si (100) surfaces, which is necessary for the growth of voids-free 3C-SiC on Si (100) substrates with a smooth interface and no obvious formation of voids on the Si side caused by the out-diffusion of Si atoms from the Si surface. The electrical properties of SiC layers were characterized by the Van der Pauw method. The room temperature Hall mobility reaches the highest value of 690cm^2/(V·s) at the carrier concentration of 3.0×10^{16}cm^{-3}. The I-V, C-V, and the temperature dependence of I-V curves in n-3C-SiC/p-Si heterojunctions with Al electrical pads were investigated. It was shown that the reverse breakdown voltage of the n-3C-SiC/p-Si heterojunction diodes reaches a maximum value of 220V. The ideal factor is 1.62 and the built-in voltage is 0.75 V. This 3C-SiC/Si heterojunction diode can be chosen for the fabrication of SiC/Si HBT's with a wide bandgap SiC emitter.

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无坑洞 n-3C-SiC/p-Si(100) 的 LPCVD 外延生长及其异质结构特性*

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摘要: 在 MBE/CVD 高真空系统上, 利用低压化学气相淀积(LPCVD)方法在直径为 50mm 的单晶 Si(100)衬底上生长出了高取向无坑洞的晶态立方相碳化硅(3C-SiC)外延材料, 利用反射高能电子衍射(RHEED)和扫描电镜(SEM)技术详细研究了 Si 衬底的碳化过程和碳化层的表面形貌, 获得了制备无坑洞 3C-SiC/Si 的优化碳化条件, 采用霍尔(Hall)测试等技术研究了外延材料的电学特性, 研究了 n-3C-SiC/p-Si 异质结的 I-V、C-V 特性及 I-V 特性对温度的依赖关系. 室温下 n-3C-SiC/p-Si 异质结二极管的最大反向击穿电压达到 220V, 该 n-3C-SiC/p-Si 异质结构可用于制备宽带隙发射极 SiC/Si HBTs 器件.

关键词: LPCVD; 无坑洞 n-3C-SiC/p-Si; 异质结特性

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