A New Structure IGBT with High Performance*

Cheng Xu[1], Wu Yu[1], Liu Xingming[1], Wang Zhe[1], Kang Baowei[1], Li Junfeng[2] and Han Zhengsheng[2]

(1 *Department of Electronics, Beijing Polytechnic University, Beijing* 100022, *China*)
(2 *Microelectronics Center, The Chinese Academy of Sciences, Beijing* 100029, *China*)

Abstract: A new structure IGBT is proposed for reducing the power dissipation. It features a composite voltage-sustaining layer which includes a n-type buffer layer formed by ultra-deep diffusion and a transparent backside emitter formed by boron implantation. Working in a deep punch-through state during its normal operating condition, it still possesses all the characteristics of the robust non-punch-through IGBT (NPT-IGBT). With a chip-thickness thinner than that of the NPT-IGBT, the new structure presents a better trade-off relationship between the on-state voltage-drop and the turn-off loss. Experimental results show that the power loss of the new structure IGBT is 40% lower than that of the NPT-IGBT.

Key words: buffer layer; deep punch through; NPT-IGBT; transparent emitter
EEACC: 2560; 2550; 1210
CLC number: TN323+.4 **Document code**: A **Article ID**: 0253-4177(2003)06-0586-06

1 Introduction

As a promising power semiconductor device, the insulated gate bipolar transistor (IGBT) has drawn special attentions recently[1~4]. The device combines the features of voltage-control in MOS devices and conductivity modulation in bipolar devices, which make the IGBT very favorable for the high-power applications.

In the course of vertical IGBT development, two typical design concepts have been proposed. In the early 1980s, the IGBT was originally invented and fabricated with the concept of punch-through (PT) type[5,6]. It is based on the n^-/n^+ two-layer epitaxy technology on a p^+ substrate. The finial device must undergo certain carrier-lifetime-killing process, such as the neutron irradiation, to obtain tolerable turn-off time and tail current. The PT-IGBT generally has two disadvantages: negative temperature coefficient of the on-state voltage-drop and great deterioration of the turn-off performance with the increase of temperature. Another concept of the non-punch-through (NPT) type IGBT was proposed at the end of the 1980s to overcome the expensive epitaxy process in the high-voltage PT-IGBT fabrication[7]. The NPT-IGBT starts from a low-cost homogeneous n^--bulk substrate. And there is no epitaxy or carrier-lifetime-killing step in its fabrication process. This kind of IGBT shows many advantages: positive temperature coefficient of on-state voltage-drop, almost unchanged turn-off characteristics with the variation of temperature, and very high ruggedness[8]. Due to the high

* Project supported by National Natural Science Foundation of China (No. 69836010)
Cheng Xu male, PhD candidate. His present research interests are in power semiconductor devices & ICs.
Kang Baowei male, professor. His present research interests are in the semiconductor physics and devices.
Han Zhengsheng male, professor. His present research interests are in deep sub-micron devices and technologies.
Received 11 December 2002, revised manuscript received 11 February 2003

performance and low product cost, the NPT-IGBT now is the mainstream in the IGBT market.

However, the performance of the NPT-IGBT can be further improved. Due to the non-punch-through state at breakdown, the NPT-IGBT needs a thicker n^--base region than the PT-IGBT for the same voltage rating. For example, the 1700V NPT-IGBT has an n^--base thickness of 280μm, while for the PT type the thickness is only 155μm. The thick n^--layer of the NPT-IGBT must be kept to ensure the low collector-emitter leakage current and the sharp breakdown characteristics[9]. But this rather thick, high resistivity n^--layer results in higher static and dynamic losses than necessary if the structure could be thinner.

This paper reports an improved structure of the voltage-sustaining layer for the 1700V IGBT in which the drawback of the thick n^--layer of NPT-IGBT is overcome. It fully takes the advantage of the punch-through concept while all the favorable features of the NPT-IGBT are still preserved. The IGBT with the new structure exhibits better performance than the PT- and NPT-IGBTs.

2　Principle of new structure IGBT

The concept for the new voltage-sustaining layer is depicted in Fig. 1 with the comparisons to the PT and NPT structure. The front-side MOSFET structures for the three types are identical. The main differences are between the voltage-sustaining layers.

As shown in Fig. 1(a), PT-IGBT has a thick and heavily doped p^+ substrate, on which two epi-layers are grown. The first layer is the n^+ buffer layer, which is about 10μm. The second layer is the thick n^--base layer. So the efficiency of the back-side p^+ emitter is very high. In the on-state, a large amount of excess carriers are stored in the n^--base region. When the device is switched off, the only way to remove these excess carriers is the carrier recombination. Therefore, in order to meet the requirement for the high turn-off speed and low turn-off losses, carrier-lifetime-killing technique must be employed. Nevertheless, the shortened carrier-lifetime leads to a negative temperature coefficient of the on-state voltage-drop that makes the parallel operation of the IGBT very complex. Furthermore, the switching speed and switching losses are also harmed from the short carrier-lifetime. As temperature goes up, the increase of the carrier-lifetime is relatively prominent. This makes the switching speed slow down thus increasing the switching losses, which might induce a vicious circle in the operation of PT-IGBT and hence harm the ruggedness.

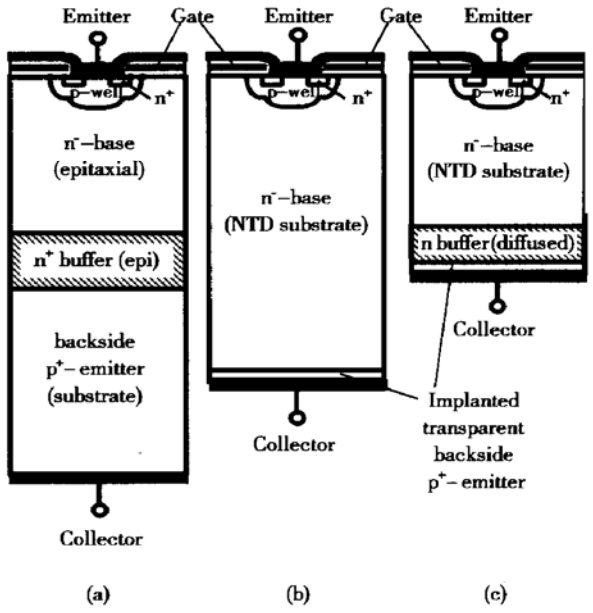

Fig. 1　Structure comparison of PT-IGBT (a), NPT-IGBT (b), and the proposed IGBT (c)

The NPT IGBT, shown in Fig. 1(b), starts, however, from a neutron-transmutation-doping (NTD) high resistivity wafer, which is much cheaper than the epitaxial wafer. One of the key points in the NPT-IGBT structure is the transparent p^+ emitter on the anode (back) side of the chip. This transparent p^+ emitter is formed by the boron implantation before the process of the back-side metalization. Hence, there is no high temperature drive-in or annealing of the implanted boron. This leads to the low activated boron-dopant and a very thin p^+ layer. These two factors guarantee a

large electron current can flow through the backside p^+ emitter (this is why this structure is called "transparent"). Therefore, during the turn-off, the stored excess carriers can be drawn out of the n^--base region through the p-wells and the transparent emitter, rather than the single way of carrier recombination in the PT case. Consequently, for NPT-IGBT, there is no need for the carrier-lifetime-killing technique. And the long carrier-lifetime can be preserved. This ensures the positive temperature coefficient of the on-state voltage-drop and the stable switching performance with the change of temperature.

In the proposed structure, as illustrated in Fig. 1(c), a buffer layer is introduced into the n^--base region (this n^--base region has a higher resistivity than that in the NPT-IGBT). The buffer layer is a residual part of a diffused layer formed by an ultra-deep diffusion at the beginning of the process. The key steps of the process flow for the new structure IGBT fabrication are shown in Fig. 2 and will be explained in the next section. Since the new structure IGBT also starts from a homogeneous high-resistivity wafer, the low cost feature is kept. And the backside p^+ emitter is also realized by the boron implantation to keep the feature of "transparent". Thus, the fast switching speed is achieved without carrier-lifetime-killing techniques. This is very critical for the positive temperature coefficient of the on-state voltage-drop and the stable switching performance.

By using the NTD wafer with a higher resistivity and above-mentioned buffer layer, the chip thickness of the new structure IGBT is reduced to 75% of that of the NPT-IGBT with the same voltage rating of 1700V, as illustrated in Fig. 1. The thinned n^--base region brings improved performance. When the IGBT is in on-state, under the same degree of conductivity modulation, the thinner thickness results in a smaller on-state voltage-drop and less stored excess carriers. The excess carrier distributions of the new structure IGBT and the NPT-IGBT in the on-state are compared in Fig. 3 which shows the numerical simulation results from Medici™. Thus, the fewer stored charges bring a shorter switching-time hence a less turn-off power loss.

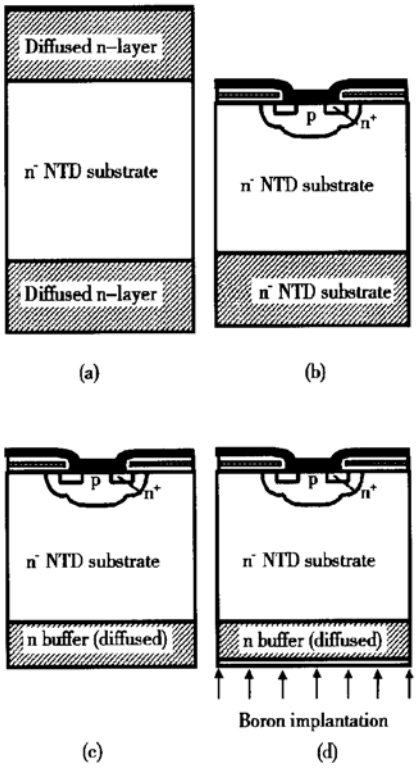

Fig. 2 Key process steps for the new-structure IGBT fabrication (a) Double-side ultra-deep phosphorus diffusion; (b) MOSFET cells fabrication after complete removal of the front side diffusion layer; (c) Grinding from backside; (d) Transparent p^+ emitter fabrication by boron implantation

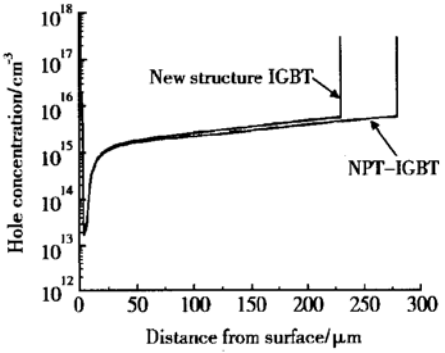

Fig. 3 Simulated excess-carrier profiles in the n^--base regions of the new structure IGBT and NPT-IGBT during on-state

3 Sample fabrication

1700V/15A new structure IGBT samples were fabricated with an area of 6.5mm × 6.5mm. The key process steps are illustrated in Fig. 2. The process started from an NTD wafer with a thickness of 550μm. Then a deep phosphorus diffusion (about 105μm) was performed from both sides of the wafer as illustrated in Fig. 2(a). After the removal of the front side diffusion layer, the MOSFET cells were fabricated on the polished front side of the wafer (Fig. 2(b)). The wafer then was ground from the backside. The residual part of the diffused layer was carefully controlled to keep a thickness of 25μm (Fig. 2(c)). Before the backside metalization, the boron was implanted into the backside of the wafer to form the p^+ emitter. The final wafer thickness is about 230μm. Figure 4 is SRP-analysis results of the net-doping profile from the backside of a fabricated sample chip.

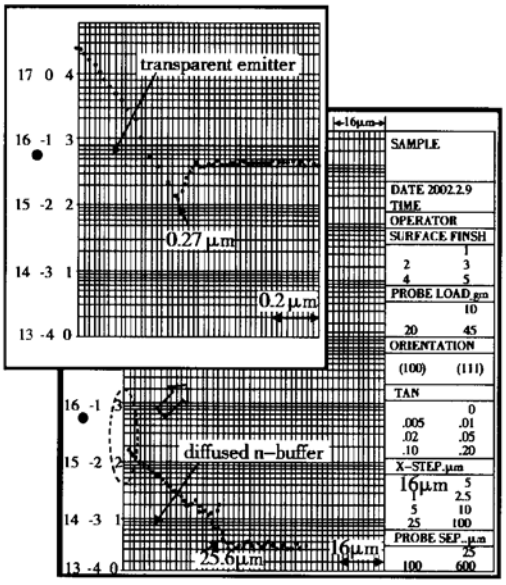

Fig. 4　Spreading resistance probing (SRP) analysis results from the backside of the fabricated sample

For comparison, the conventional NPT-IGBT samples with same die area were also fabricated. The process for NPT-IGBT was quite similar to the new structure IGBT except that there was no deep phosphorus diffusion at the beginning of the process. The final thickness of a wafer for the NPT-IGBT was about 280μm.

4 Measured results

Figure 5 shows the collector-emitter breakdown curves for the new structure IGBT and NPT IGBT samples. As can be seen, there is no apparent difference between the two types. Figure 6 shows the typical inductive switching-off waveforms of the new structure IGBT under 1100V/15A. The current drops very fast and the tail current is almost unnoticeable. The measured trade-off curves for the two types are compared in Fig. 7. It can be seen that, at the same turn-off losses, the on-state voltage-drop of the new structure IGBT is almost 40% lower than that of the NPT-IGBT. Mean-

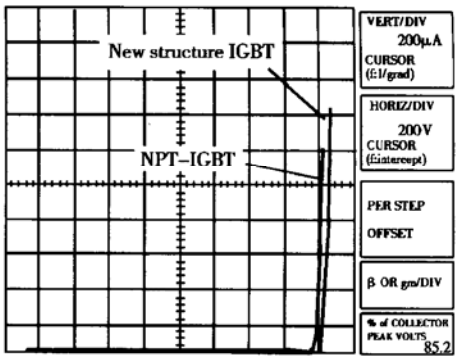

Fig. 5　Measured collector-emitter breakdown curves of the fabricated new-structure IGBT sample and the fabricated NPT-IGBT sample

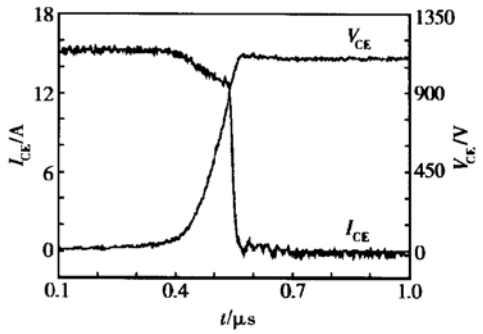

Fig. 6　Measured inductive turn-off curves of the fabricated new-structure IGBT sample with V_{CC} = 1100V, I_C = 15A, L = 3mH, R_g = 150Ω

while, the positive temperature coefficient of the on-state voltage-drop is achieved. For the new structure IGBT, the measurements show that the on-state voltage-drop increases 14.8% when the ambient temperature increases from 25℃ to 125℃. The new structure IGBT also exhibits a stable switching performance. As the temperature rises from 25℃ to 125℃, only minor variation of the switching performance can be observed. Therefore, the new structure IGBT dissipates lower power loss than NPT-IGBT while still preserving the positive temperature coefficient of the on-state voltage-drop and the stable switching performance.

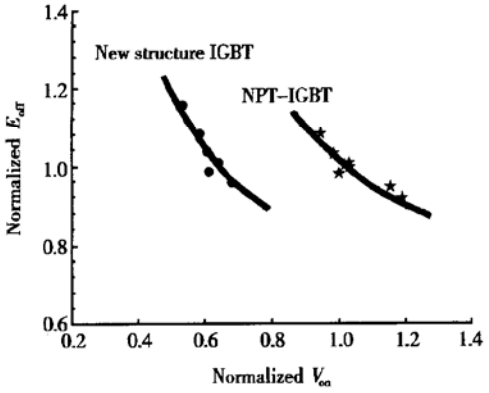

Fig. 7 Trade-off curves for the new structure IGBT and NPT-IGBT

5 Conclusion

A new structure 1700V/15A IGBT is demonstrated in this paper. It features a novel voltage-sustaining layer which includes a residual layer of a pre-diffused n-type layer and a transparent back-side p^+ emitter formed by implantation. The fabricated samples have shown a 40% reduction in the power loss when comparing with the NPT-IGBT. It remains a positive temperature coefficient of the on-state voltage-drop, and its switching performance changes very little with the variation of the temperature. This new structure is a good candidate for the next generation of high-performance IGBTs.

References

[1] He Jin, Wang Xin, Chen Xingbi. Preparation of PT-IGBT with new structure based on SDB. Chinese Journal of Semiconductors, 2000, 21: 877(in Chinese) [何进, 王新, 陈星弼. 基于SDB技术的新结构PT型IGBT器件研制. 半导体学报, 2000, 21: 877]

[2] Wu Yu, Lu Xiuhong, Kang Baowei, et al. A novel low power loss IGBT (LPL-IGBT) and its simulation. Chinese Journal of Semiconductors, 2002, 23: 1565(in Chinese) [吴郁, 陆秀洪, 亢宝位, 等. 低功耗IGBT(LPL-IGBT)及其仿真. 半导体学报, 2002, 23: 1565]

[3] Yang Hongqiang, Chen Xingbi. A high speed IGBT based on dynamic controlled anode-short. Chinese Journal of Semiconductors, 2002, 23: 1014

[4] Yang Hongqiang, Han Lei, Chen Xingbi. Improvement of electrical performance of SOI-LIGBT by resistive field plate. Chinese Journal of Semiconductors, 2002, 23: 1565

[5] Baliga B J, Adler M S, Gray P V, et al. The insulated gate rectifier (IGR): a new power switching device. IEEE Electron Devices Meeting Digest, 1982: 264

[6] Russell J P, Goodman A M, Goodman L A, et al. The COMFET: a new high conductance MOS gated device. IEEE Electron Device Lett, 1983, 4: 63

[7] Miller G, Sack J. A new concept for a non punch through IGBT with MOSFET like switching characteristics. 20th Annual IEEE Power Electronics Specialists Conference (PESC'89) Record I, 1989: 21

[8] Laska T, Miller G, Niedermeyer J. 2000V-non-punch-through IGBT with high ruggedness. Solid-State Electron, 1992, 35 (5): 681

[9] Takahashi Yoshikazu, Yoshikawa Koh, Koga Takeharu, et al. Experimental investigations of 2.5kV-100A PT type and NPT type IGBTs. Proceedings of 1995 International Symposium on Power Semiconductor Devices and ICs, 1995: 70

一种高性能的新结构 IGBT*

程　序[1]　吴　郁[1]　刘兴明[1]　王　哲[1]　亢宝位[1]　李俊峰[2]　韩郑生[2]

(1 北京工业大学电子工程系，北京　100022)

(2 中国科学院微电子中心，北京　100029)

摘要：提出了一种低功率损耗的新结构 IGBT. 该新结构的创新点在于其复合耐压层结构，该耐压层包括深扩散形成的 n 型缓冲层和硼注入形成的透明背发射区两部分. 虽然在正常工作条件下，该新结构 IGBT 工作于穿通状态，但器件仍具有非穿通 IGBT(NPT-IGBT)的优良特性. 该新结构 IGBT 具有比 NPT-IGBT 更薄的芯片厚度，从而可以获得更好的通态压降和关断功耗之间的折衷. 实验结果表明：与 NPT-IGBT 相比较，新结构 IGBT 的功率损耗降低了 40%.

关键词：缓冲层；深穿通；NPT-IGBT；透明发射区

EEACC：2560；2550；1210

中图分类号：TN323+.4　　**文献标识码**：A　　**文章编号**：0253-4177(2003)06-0586-06

* 国家自然科学基金资助项目(批准号：69836010)

程　序　男，博士研究生，目前主要从事功率半导体器件和集成电路方面的研究.

亢宝位　男，教授，博士生导师，目前主要从事半导体器件和器件物理方面的研究.

韩郑生　男，教授，博士生导师，目前主要从事深亚微米器件和工艺方面的研究.

2002-12-11 收到，2003-02-11 定稿