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An Improved Method to Extract Generation of Interface Trap in Hot-Carrier-Stressed LDD n-MOSFET*

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Abstract: A new improved technique, based on the direct-current current-voltage and charge pumping methods, is proposed for measurements of interface traps density in the channel and the drain region for LDD n-MOSFET. This technique can be applied to virgin samples and those subjected to hot carrier stress, and the latter are known to cause the interface damage in the drain region and the channel region. The generation of interface traps density in the channel region and in the drain region can be clearly distinguished by using this technique.

Key words: hot-carrier stress; LDD; ultra-thin gate oxide; two-step degradation

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1 Introduction

The hot-carrier induced devices and circuits degradation is an important reliability constraint for ULSI[1~3]. It has been long known that the mechanism responsible for the device degradation in n-MOSFET is interface-state generation. And for LDD n-MOSFET, it has been widely reported[4~9] that the saturation in time dependence of the degradation is due to the combination of an increase in the series resistance in the LDD region, and a reduction of the carrier mobility in the channel. The series resistance degradation is directly related to the number of interface states generated in the drain region: $\Delta N_{it,d}$, while the carrier mobility degradation is directly related to the number of interface states generated in the channel region: $\Delta N_{it,c}$. It is well established that hot carrier degradation of n-channel MOSFETs follows a time power-law relationship $\Delta g_m = At^n$, where Δg_m is the percentage change in transconductance with respect to unstressed device, A and n are coefficients, and t is degradation time. A two stage saturating/self-limiting behavior, observed during long stress periods, has been commonly attributed to the combination of saturating series resistance and decreasing channel mobility.

Many methods are proposed to study the interface traps generated in the channel and the interface

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traps generated in the drain region, in which the charge pumping technique is an important one[7,8,10~12]. However, along with the reduction of device dimensions, the assumption that a uniform interface state density exists for a virgin device may be not always valid due to varying extents of damage sustained from ion implantation and high tensile stress near channel edges[8]. In order to overcome the limitations, an improved method is necessary to develop.

Recently, direct-current current-voltage (DCIV) technique is proposed to extract the information about interface trap generation, and it is reported that this method is easy to separate the interface state generation in the drain region and the channel region[13~16]. Unfortunately, while oxide thickness is becoming thin, due to the p-n junction leakage and trap-assisted-tunneling (TAT) existence, it is difficult to observe the DCIV peak near the drain, although the peak in channel is always observed.

Therefore, in this paper, we propose a new method to separate the interface state generation in the drain region and the channel region by combining both charge pumping and DCIV for ultrathin gate oxide n-MOSFET under hot-carrier stress.

2 Methods

2.1 Charge pumping method

In the charge pumping (CP) measurements[17,18], trapezoidal pulses are applied to the gate of the device, with the junction of interest and the substrate grounded and the other junction left floating. The base voltage of the pulse, V_B, is kept constant and below the flatband voltage V_{FB} of the channel, while the high level of the pulse V_H is being swept. Since the charge pumping current arises from the recombination of electrons with holes via interface traps over a pulse cycle, only those regions that undergo accumulation-inversion-accumulation (or inversion-accumulation-inversion) over a pulse cycle contribute to the charge pumping current. In other words, for a given pulse cycle, only those interface traps in regions where the local V_{FB} is higher than V_B and the local V_t is lower than V_H can contribute to the charge pumping current measured at the junction of interest. The charge pumping current, I_{CP}, saturates as V_H exceeds the maximum V_t in the channel and this current ($I_{CP,max}$) arises from all the interface traps distributed throughout the gate length, provided V_B is sufficiently low. And the $I_{CP,max}$ is given by:

$$I_{CP,max} = qfN_{it,total}WL \tag{1}$$

where q is electron charge, f frequency of the pulse, W mask channel width, and L effective length for CP measurements.

According to the CP theory, for a LDD n-MOSFET we can obtain:

$$I_{CP}(V_{g0}) = qfN_{it,d}WL \tag{2}$$

where V_{g0} is the value of gate voltage which make the surface potential in the junction of drain equals to V_t.

Then the N_{it} in the channel region is given as

$$I_{CP,max} - I_{CP}(V_{g0}) = qfN_{it,c}WL \tag{3}$$

2.2 DCIV method

In DCIV measurements, it is generally found that the substrate current (I_B) versus gate voltage (V_g) plot consists of two peaks, one corresponding to the recombination current via interface traps in the channel region, and the other corresponding to that in the drain region. The height of the substrate current peak ($I_{B\text{-}peak}$) is directly proportional to the interface trap density, which can be calculated using the following formula:

$$\Delta N_{it,c}/N_{it,c} = (I^{c}_{B\text{-}peak,final} - I^{c}_{B\text{-}peak,initial})/I^{c}_{B\text{-}peak,initial} \tag{4}$$

$$\Delta N_{it,d}/N_{it,d} = (I^{d}_{B\text{-}peak,final} - I^{d}_{B\text{-}peak,initial})/I^{d}_{B\text{-}peak,initial} \tag{5}$$

where $I^{c}_{B\text{-}peak}$ and $I^{d}_{B\text{-}peak}$ are the peak height of the base current (I_B) corresponding to the channel and the drain region, respectively.

With the reduction of gate oxide thickness, it is difficult to detect the peak of I_B in the drain region, although the initial peak of base currents in both regions are observed, which are due to the role of leakage current of p-n junction and TAT current. The re-

combination current I_B is masked when interface traps are generated. Figure 1 shows the DCIV curves under hot-carrier stress ($V_g = V_d/2 = 1.8V$) with stress time varied from initial to 1200s. After hot-carrier stress, no obvious peak of I_B in drain region is observed.

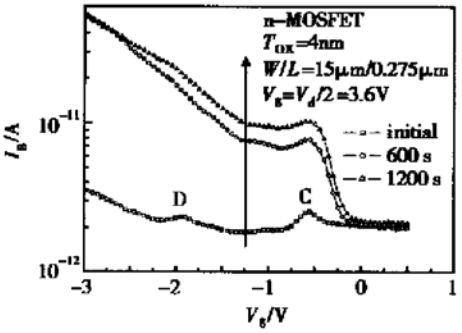

Fig. 1　DCIV curves under hot-carrier stress with stress time varied from initial to 1200s

2.3　Improved method

In this paper, we propose a method to determine $\Delta N_{it,c}$ and $\Delta N_{it,d}$ by combining both the CP and DCIV techniques. According to the Eqs. (1) and (4), we have

$$\frac{\Delta N_{it,c}/N_{it,c0}}{\Delta N_{it,total}/N_{it,total0}} = \frac{\Delta I^c_{B,peak}/I^c_{B,peak0}}{\Delta I_{CP,max}/I_{CP,max0}} = \alpha \quad (6)$$

Since $N_{it,c0}$ and $N_{it,total0}$ are constant, the proportionality of $\Delta N_{it,c}$ to $\Delta N_{it,total}$ and the degradation mechanism can be qualitatively studied by the determination of α.

And more, according to Eqs. (2) and (4), we have

$$\Delta N_{it,c}/N_{it,c} = \Delta I^c_{B,peak}/I^c_{B,peak0} = \Delta I_{CP}(V_{g0})/I_{CP0}(V_{g0}) \quad (7)$$

Once the value of $\Delta I^c_{B,peak}/I^c_{B,peak0}$ is determined by DCIV measurements, we can extract the value of V_{g0} from the curve of CP measurements. Then, the generated $\Delta N_{it,c}$ in the channel and $\Delta N_{it,d}$ in the drain region can be separated easily.

The n-channel MOSFETs used in this study are fabricated using a 0.25μm process with conventional LDD structures. The MOSFET dimensions are T_{ox}= 4nm, W= 15μm, and L= 0.275μm for all measurements in our study.

Hot-carrier stressing is performed for drain voltages V_d of 3.6V and the gate voltages varied from 0.5V to 3.6V. The source and bulk terminals of the device are grounded during stressing.

Generation of interface traps is monitored by the CP technique and DCIV method. Charge pumping pulses have a frequency of 500kHz, 50% duty cycle, rise/fall times of 150ns each and a fixed base voltage of −2.5V. In DCIV measurements, the source is connected to a high-resistor, the substrate is grounded, and the junction between the substrate and the drain is forward-biased (= 0.3V), while the surface potential is controlled by the swept gate voltage (V_g).

3　Results and discussion

Figure 2 shows the time evolution of DCIV current versus the time evolution of charge pumping current under hot-carrier stress for different gate stress voltages. The stress-induced damage under hot-carrier stress is nonuniform in spatial distribution and is located both in channel region and drain region. It can be observed that, when gate stress voltage increases, the damage located in the channel region plays a more important role.

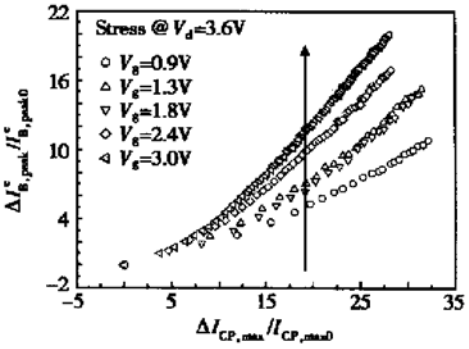

Fig. 2　Relation between $\Delta I^c_{B,peak}/I^c_{B,peak0}$ and $\Delta I_{CP,max}/I_{CP,max0}$

To be clear, we plot the change of coefficient α versus stress time in Fig. 3. Obviously, with the increase of stress time, α increases and saturates.

From Figs. 2 and 3, we can observe that when stress time increases, the N_{it} generates firstly in the drain region, and then changes to the channel. The

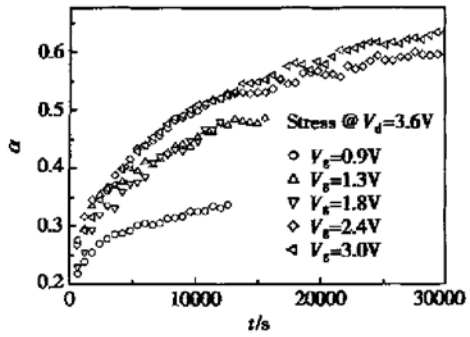

Fig. 3 Time dependence of α under hot-carrier stress for different gate stress voltages

higher the gate stress voltage is, the more the N_{it} generates in the channel region.

The method is applied for a sample stressed at V_g= 1.8V and V_d= 3.6V (V_g= V_d/2 mode). And the extracted V_{g0} is - 0.5V and - 0.2V for pre stress and after stress, respectively. The change of V_{g0} before and after stress is due to the generation of hot-carrier-induced traps, which cause the interface traps located at near drain junction to be easily detected by the charge pumping measurements.

Figure 4 (a) shows the evolution of $N_{it,c}$ and $N_{it,d}$, which are determined by this method. With the increase of stress time, both $N_{it,c}$ and $N_{it,d}$ increase. It is observed that the $N_{it,d}$ is saturated, while $N_{it,c}$ continues to increase and agrees with power-law.

And in Fig. 4 (b) the $N_{it,c}/N_{it,total}$ and $N_{it,d}/N_{it,total}$ are also given. It is clearly seen that $N_{it,d}/N_{it,total}$ gradually decrease, while $N_{it,c}/N_{it,total}$ continues to increase during stress, which indicates the generation of interface traps move from the drain to the channel region.

The method is applied for different samples under different hot-carrier stress conditions, and the value of V_{g0} is extracted and shown in Table 1.

From Table 1, the value of V_{g0} is independent of stress conditions. However, It is dependent on the location of device in the wafer. For the same location of X, the V_{g0} is nearly the same, whatever at pre stress and after stress. The results in Table 1 indicate that our method is valid.

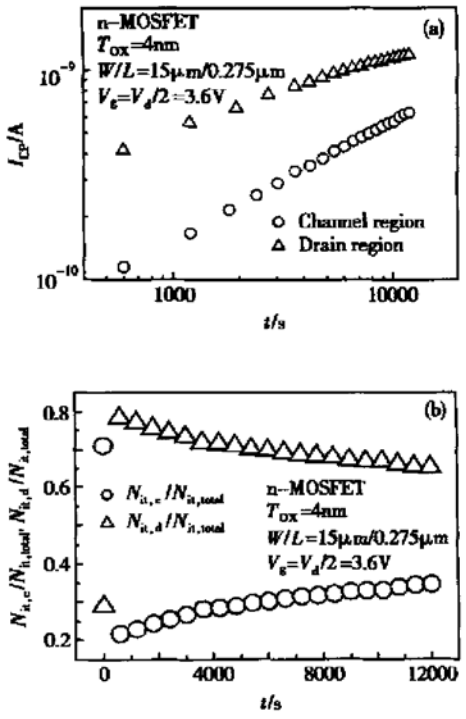

Fig. 4 (a) Time evolution of interface traps (I_{CP}) in the channel region and drain region; (b) Comparison between $N_{it,c}/N_{it,total}$ and $N_{it,d}/N_{it,total}$ with stress time varied

Table 1 Extraction of V_{g0} V

Location	X3Y4	X3Y5	X3Y6	X5Y3	X5Y4	X5Y5
Stress conditions	V_g= 1.8 V_d= 3.6	V_g= 0.5 V_d= 3.6	V_g= 0.9 V_d= 3.6	V_g= 1.3 V_d= 3.6	V_g= 2.4 V_d= 3.6	V_g= 3.0 V_d= 3.6
V_{g0}(pre stress)	- 0.5	- 0.5	- 0.6	- 0.9	- 0.9	- 0.8
V_{g0}(after stress)	- 0.2	- 0.2	- 0.2	- 0.3	- 0.3	- 0.3

Figure 5 shows the time evolution of $N_{it,c}$ and $N_{it,d}$ for LDD n-MOSFET under different stress conditions. It is observed that for different stress conditions, all time dependence of $N_{it,c}$ agree well with power-law, and all time dependence of $N_{it,d}$ are saturated.

In the early study, the injection of energetic carriers into the gate oxide has long been regarded as the only mechanism responsible for generating interface traps during hot-carrier stress[19,20]. However, by comparing the interface immunity of deuterium-annealed and hydrogen-annealed devices, some recent works[21] show that a much lower N_{it} generation pro-

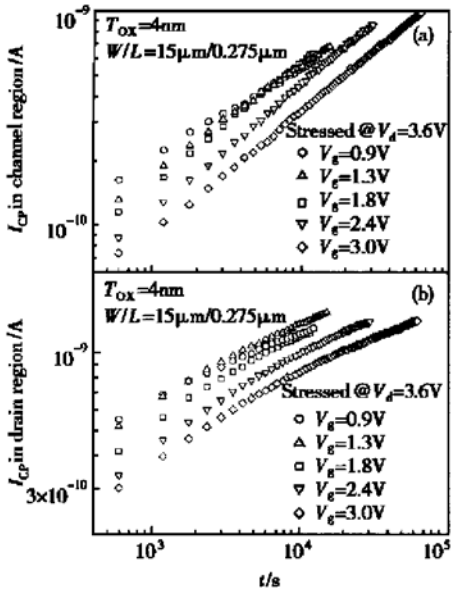

Fig. 5　Time evolution of $N_{it,c}$(a), and $N_{it,d}$(b) for different hot-carrier stress conditions

cess was found in deuterium-annealed devices during hot-carrier stress. Both devices, however, showed similar N_{it} generation under purely hot-hole or hot electron injection condition. The absence of isotopes effect in the latter seems to suggest that N_{it} generation during hot-carrier stress is not directly caused by charge injection into the gate oxide.

Recently, Ang[22] examined hot-carrier induced N_{it} generation and suggested the possible existence of two distinct N_{it} generation processes. One process is indeed correlated to the type of hot carriers injected into the gate oxide, and only dominates during the early stress stage. The other process, which proceeds with a higher generation coefficient, is found to dominate N_{it} generation in the late stress stage, and would probably determine the overall lifetime of the devices. It is shown that the interface damage associated with this process first initiates near the spacer region, and subsequently propagates into the gate-to-drain overlap and channel regions as stress progresses.

In Fig. 5, the time evolution of $N_{it,c}$ and $N_{it,d}$ under different hot-carrier stress conditions supports the two-step degradation mechanism[21,22] for LDD n-MOSFET.

In our method, we use the DCIV measurements to obtain accurate information of interface traps in channel, and use CP measurements to obtain the total interface traps in the channel and the drain region. Then combining both techniques, we can separate and determine the interface traps in the channel and in drain region. And more, in our method, a technique of ratio is used to extract $\Delta N_{it,c}/N_{it,c}$, and avoid the complex of determination of coefficient in following equation[23]

$$I_B = \frac{qN_{it}C_e^t n_i^2(\exp(qV_{EB}/kT) - 1)}{n_0\exp(q\Psi_s/kT) + p_0\exp[-q(\Psi_s - V_{EB})/kT] + 2n_i}$$

All the above discussion shows that our method is a useful tool to determine the interface traps in the channel and in the drain region.

4 Conclusion

We propose a new method to experimentally determine the interface traps generated in the channel region and in the drain region for LDD n-MOSFETs with ultrathin gate oxide thickness under hot-carrier stress. Based on this method, we compare the time evolution of N_{it} in two regions under different stress conditions. And the degradation mechanism under hot-carrier stress is studied. Finally, the method is validated by our experimented results.

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一种用于提取 LDD 结构 n-MOSFET 热载流子应力下界面陷阱产生的改进方法*

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摘要: 提出了一种新的基于电荷泵技术和直流电流法的改进方法,用于提取 LDD n-MOSFET 沟道区与漏区的界面陷阱产生.这种方法对于初始样品以及热载流子应力退化后的样品都适用.采用这种方法可以准确地确定界面陷阱在沟道区与漏区的产生,从而有利于更深入地研究 LDD 结构器件的退化机制.

关键词: 热载流子应力; LDD 结构; 超薄栅氧化层; 两步退化机制

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