Distortion Behavior for SOI MOSFET*

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Abstract: Distortion analysis of SOI MOS transistor is presented. By the power series method, the distortion behaviors of FD (fully depleted) and RC (recessed channel) SOI MOS transistor configurations are investigated. It is shown that the distortion figures deteriorate with the scaling down of channel length, and the RC SOI device shows better distortion performance than the FD SOI device. At the same time, the experimental data show that the ineffective body contact can lead to an increase of the harmonic amplitude due to the bulk resistance. The presented results give an intuitive knowledge for the design of low distortion mixed-signal integrated system.

Key words: distortion behavior; power series method; SOI MOSFET
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1 Introduction

SOI MOS transistor is used in modern mixed-signal system because it can work beyond the limit in current silicon technology in terms of power consumption, circuit density, operation speed, and scaling limit[1]. However, due to the nonlinearity of SOI MOSFET, the harmonic distortion becomes a key issue. The nonlinear effect, together with the noise, increases the unwanted signal in high precision analog circuit such as RF integrated transceivers[2], integrated g_m-C filter[3], CMOS mixers[4], and degrade the performance of circuit. For the accurate design of SOI MOSFET-based analog circuit, an intuitive knowledge of the distortion behavior of SOI single transistor is indispensable. Although several authors have studied the nonlinear behavior of bulk MOSFET[5~7], little attention has been paid to the nonlinear behavior of SOI single transistor, especially, the systematical comparison between different SOI MOSFET configurations. Based on these backgrounds, Zhang *et al.*[8] presented a SOI-based physical distortion model, and this model can give a better description of the distortion behavior of SOI MOSFET.

In this paper, the distortion analysis of FD (fully depleted) and RC (recessed channel) SOI MOSFET are experimentally investigated. To meet the demand of distortion analysis, SOI MOS transistor is assumed working in strong inversion and weakly nonlinear regime which is the typical working situation for the analogous applications. With this assumption the nonlinear element of SOI MOS transistor can be described by power series. The coefficients in these power se-

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ries, which are computed by obtaining higher order derivatives from the measured DC current-voltage characteristic, are used to describe the harmonic distortion behavior of the device. From the analysis of the experimental results, we can see that RC SOI structure due to its low source-drain resistance has a lower distortion figure than the FD SOI, and serves as a primo-candidate for the low distortion application.

2 Experiment and measurement

The measurements presented here were done on n-type FD and RC SOI MOSFETs with and without body contact. The body was linked through the metal contact at one end of channel width which will bring bulk distributed resistance. The channel width was 10μm and the length was changed. The gate oxide thickness was about 11nm. The DC I_{ds}-V_{gs} and I_{ds}-V_{ds} data were obtained from HP4145B semiconductor parameter analyzer. According to the power series method, the nonlinear element in single transistor can be studied by a small excursion around a quiescent point, and the excursion is often described as a power series of the algebraic function, in which the derivatives are computed in the quiescent point:

$$i_{ds} = k_0 + k_1 v_i + k_2 v_i^2 + k_3 v_i^3 + \cdots = \sum_{n=0}^{\infty} k_n v_i^n$$

where $k_0 = I_{ds}$, $k_1 = \frac{\partial I_{ds}}{\partial V} \mid_{V_{ds0} \text{ or } V_{gs0}}$, $k_2 = \frac{1}{2!} \times \frac{\partial^2 I_{ds}}{\partial V^2} \mid_{V_{ds0} \text{ or } V_{gs0}}$, $k_3 = \frac{1}{3!} \times \frac{\partial^3 I_{ds}}{\partial V^3} \mid_{V_{ds0} \text{ or } V_{gs0}}$, V is the terminal voltage, v_i is input signal, I_{ds} is the DC current and k_n is higher order derivative or nonlinear coefficient. If the amplitude of the input signal is not too large, the amplitude of the higher-order harmonics corresponds to the higher order nonlinear coefficients of the power series[9]. So, by doing numerical differentiation towards the measured DC I-V characteristics, the amplitude of harmonic distortion can be obtained. However, more attention should be paid to the numerical noise induced by the differentiation. In this analysis, multi-point local polynomial smoothing process was adopted to reduce the numerical noise, and good results were obtained.

3 Results and discussion

SOI MOS transistors in non-saturation strong inversion conditions were used as tunable linear resistors in filter applications. The major limitation of the technique lies in the generation of third-order harmonic distortion. Figure 1 shows the amplitude of the gate-voltage-induced third order harmonic distortion for FD devices with L = 10μm and 0.6μm respectively at V_{ds} = 0.1V. For a long channel device with L = 10μm, the series resistance effect is negligible and the distortion behavior is mainly affected by mobility

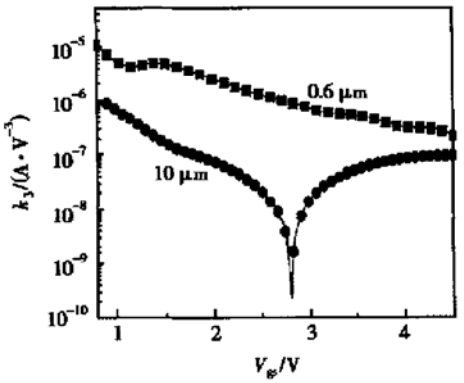

Fig. 1 Comparison of third order gate-voltage-induced distortion behavior for L = 10μm and 0.6μm at V_{ds} = 0.1V

degradation. According to Ref. [10], the sharper transition from the phonon scattering limited carrier mobility to the surface roughness scattering limited carrier mobility induces the zero-crossing. When the channel length reduces to 0.6μm, the series resistance effect makes the amplitude of the third order harmonic distortion larger and the nonlinear behavior becomes worse. Figure 2 shows the third order distortion behavior with the same structural and technological parameters as those of Fig. 1, but at different V_{ds}, namely V_{ds} = 2V. When keeping the drain voltage constant, device will experience a transition from the saturation region to linear region with the increase of V_{gs}. The dashed line in Fig. 2 indicates the transition point. As illustrated in Fig. 2, the largest amplitude of

harmonic distortion moves towards the smaller gate voltage with the scaling down of channel length. This makes the low-distortion characteristic under lower voltage worse for shorter channel transistors.

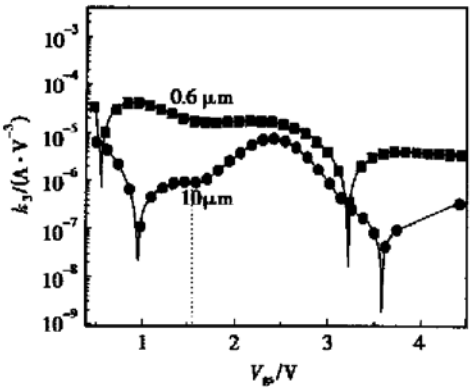

Fig. 2 Comparison of third order gate-voltage-induced distortion behavior for $L = 10\mu m$ and $0.6\mu m$ at $V_{ds} = 2V$

The third order drain-voltage-induced distortion of FD SOI devices ($L = 0.6\mu m$ and $V_{gs} - V_{th} = 1.5V$) is given in Fig. 3. In FD SOI transistors, the full depletion gives the silicon below the gate an al-

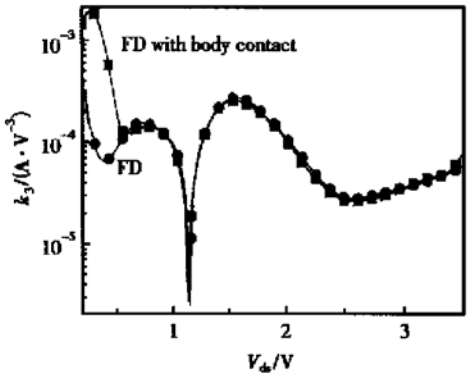

Fig. 3 Comparison of third order drain-voltage-induced distortion behavior for FD floating body and body contact with $L = 0.6\mu m$ at $V_{gs} - V_{th} = 1.5V$

most infinite resistivity. From the comparison of the third order harmonic distortion between FD devices with and without body contact, we can find that body contact does not change the distortion behavior too much except for the increase of distortion in linear region. The possible reason is the resistance induced by the body contact of FD device.

Figure 4 shows the comparative result of the gate-voltage-induced third order harmonic distortion of FD and RC SOI MOSFETs ($L = 0.6\mu m$ and $V_{ds} = 0.1V$). It can be seen that the amplitude of the third order harmonic distortion of RC structure is lower than that of the FD due to the reduced series resistance in the raised source-drain region, and it can also be explained by the SOI distortion model in Ref. [8]. Figure 5 illustrates the distortion behavior of the drain-voltage-induced third order distortion of FD and RC SOI MOSFETs with $L = 0.6\mu m$ and $V_{gs} - V_{th} = 1.5V$, and it can be seen that RC structure shows better distortion behavior owing to the optimized source and drain elevation.

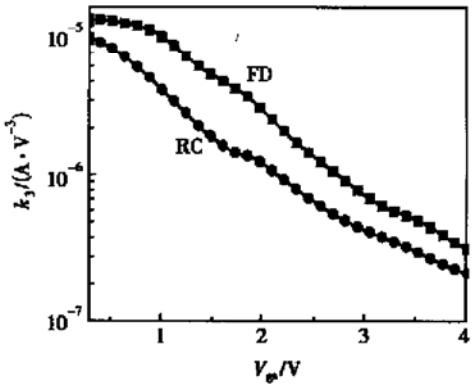

Fig. 4 Comparison of third order gate-voltage-induced distortion behavior for FD and RC structures with $L = 0.6\mu m$ at $V_{ds} = 0.1V$

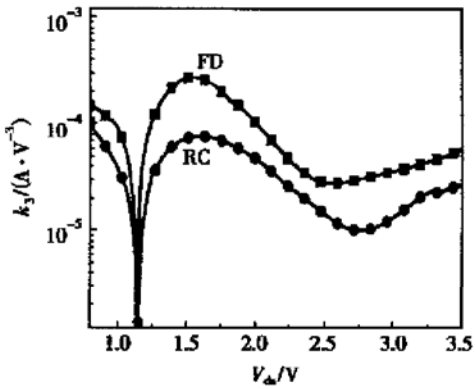

Fig. 5 Comparison of third order drain-voltage-induced distortion behavior for $L = 0.6\mu m$ at $V_{gs} - V_{th} = 1.5V$

4 Conclusion

This work has analyzed the distortion behavior of different SOI MOS transistor configurations including FD and RC SOI devices. The analysis show that the amplitude of harmonic distortion becomes worse as the channel length is reduced, and FD device has a worse distortion behavior in linear region because of the body distributed resistance. Besides, RC device can decrease the distortion amplitude and increase the linearity due to the elevated source and drain structure. The presented results can give the circuit designers an intuitive knowledge during the low distortion analogous integrated circuit application.

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SOI MOSFET 的失真行为*

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摘要: 采用幂级数方法对基于全耗尽(FD)SOI MOSFET 和凹陷(RC)沟道 SOI MOSFET 的失真行为进行了研究, 发现随着沟道长度的减小失真行为变坏, 且 RC SOI 器件较 FD 器件具有更好的失真行为. 同时, 从实验数据可以看出, 不理想的体接触会由于体分布电阻的增加而使失真行为变坏. 该结果可以为低失真混合信号集成系统的设计提高指导方向.

关键词: 失真行为; 幂级数; SOI MOSFET

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