

## 0.6 $\mu$ m CMOS Laser Diode Driver for Optical Access Networks\*

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**Abstract:** Using native CMOS technology, EDA tool, and adopting full custom design methodology, a laser diode driver for the use of STM-1 and STM-4 optical access network, is realized by CSMC-HJ 0.6 $\mu$ m CMOS technology to modulate laser diodes at 155Mb/s (STM-1), 622Mb/s (STM-4) with adjustable modulation current from 0 to 50mA for an equivalent 50 $\Omega$  load. The maximum modulation voltage is over 2.5V<sub>pp</sub> corresponding to a 3V DC bias for output stage. The time range of rise and fall from 360ps to 471ps is measured from the output voltage pulse. The RMS jitter is no more than 30ps for four bit rates. The power consumption is less than 410mW under a power supply voltage of 5V. According to the experimental results, the laser diode driver achieves the same level as their counterparts worldwide.

**Key words:** laser diode driver; CMOS; optical access networks

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### 1 Introduction

With the rapid development of optical networks, super performance and low cost of optical transmitters are needed<sup>[1,2]</sup>. The best choice to realize such optical transmitters is through CMOS technology. CMOS technologies are playing an increasingly important role in super performance ICs for the use of optical fiber communications due to the low cost and the great progress of CMOS technology itself<sup>[3,4]</sup>. In the past years, other laser diode driver was realized through InP-based technology<sup>[5]</sup> within China mainland. However, for the low cost commercial application of optical access network operating at low data speed,

in this work, a laser diode driver was realized by CSMC-HJ 0.6 $\mu$ m CMOS technology, which can meet the requirement of 155Mb/s and 622Mb/s optical transmitters.

### 2 Circuit design and simulation

The schematic diagram of the circuit is shown in Fig. 1. The DC coupled, fully differential circuit consists of an input buffer, two amplifying stages and an output stage. The whole circuit is fully balanced by employing differential amplifiers to maximize its work speed.

The upper NMOS transistor pair in each amplifying stage is a differential current amplifier. The lower transistor forms the current source for the NMOS transistor pair.

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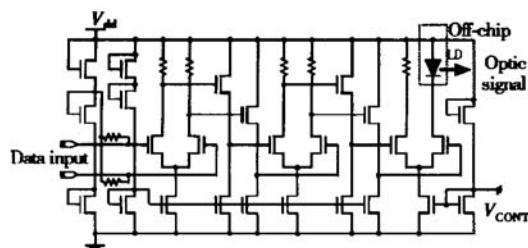


Fig. 1 Schematic diagram of laser diode driver circuit

The resistor pair is adopted as loads. A differential source follower is employed to realize the functions of level-shifting and impedance transforming. The input and output buffers provide the function of impedance matching and DC level matching. In this work, conventional poly resistors, which were introduced to divide the supply voltage  $V_{DD}$  into internal reference voltage  $V_{REF}$  for the use of DC bias of current sources, were replaced by multiple diode-connected NMOS transistors because a more accurate DC bias voltage for current sources can be obtained by using diode-connected NMOS transistors than that of poly resistors because of their large resistance error resulting from inevitable process variation.

Due to very large output current swing of the LD driver, most of the devices have large aspect ratios ( $W/L$ ). This will necessarily result in increased parasitic capacitance, especially in critical nodes, which strongly impacts the high speed operation of the laser diode driver<sup>[6]</sup>. Multiple-finger structure offering nearly 50% reduced source and the drain area was employed for all large transistors to minimize parasitic capacitance. Special attention has been given to keep routes as short as possible while using large width to meet the requirement of current density and to minimize parasitic inductance. Great care also has been taken as to virtually avoid large area overlap between supply and signal lines. For the purpose of effective biasing and minimization of substrate bouncing, substrate contact arrays have been extensively used. In addition, double metals which composed ground lines and other DC supply lines were used in large area as MIM (metal-insulator-metal) capacitors to cancel undesired noises. Therefore, the performance of this circuit was better in great degree due to all design techniques mentioned above.

### 3 Circuit fabrication

The laser diode driver was designed using 0.6 $\mu$ m double-poly double-metal N-well CMOS technology and fabricated in Wuxi CSMC-HJ Semiconductor Co., Ltd. The chip microphotograph of the die is shown in Fig. 2. The chip dimensions including bonding pads are 0.7mm  $\times$  1.0mm. On the chip, only one tenth of the total chip area in the middle region was used for the active part.

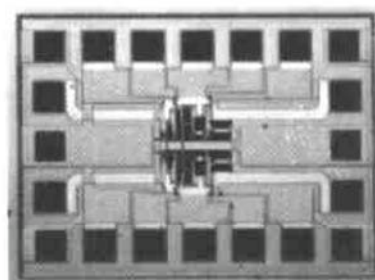


Fig. 2 Microphotograph of the fabricated CMOS laser diode driver

A very important fact should be pointed out that the chips for the use of optical transmitters in optical access networks were realized within China mainland all by native resources such as PANDA system, a layout EDA software of CIDC (China Integrated Circuit Design Center), IC manufacturing line of Wuxi CSMC-HJ Semiconductor Co., Ltd. All design kits were developed by IROI (Institute of RF- & OE- ICs.), Southeast University and the support from the MPW plan of Shanghai ICC.

### 4 Experimental results

The performance of the fabricated laser diode driver was evaluated via on-wafer probing on uncut wafers employing CASCADE MICROTECH probe station, an ADVANTEST D3186 Pulse Pattern Generator, an ADVANTEST R6142 Programmable DC Voltage/Current Generator, a ROHDE & SCHWARZ SMP04 Signal Generator (10MHz~40GHz) and an Agilent Infinium DCA 86100A Wide-bandwidth Oscilloscope. The DC current of the laser diode driver under a supply voltage of 5V was less than 82mA, corresponding to a power dissipation of 410mW.

The circuit was tested using an input PECL of 500mV<sub>pp</sub> at different bit rates. The measured eye diagrams at the bit rates of 155, 622, 1250, and 1600Mb/s from one single-

ended output of the laser driver are shown in Figs. 3 (a), (b), (c), and (d). The modulation current range at each single-end output is 0~ 50mA.

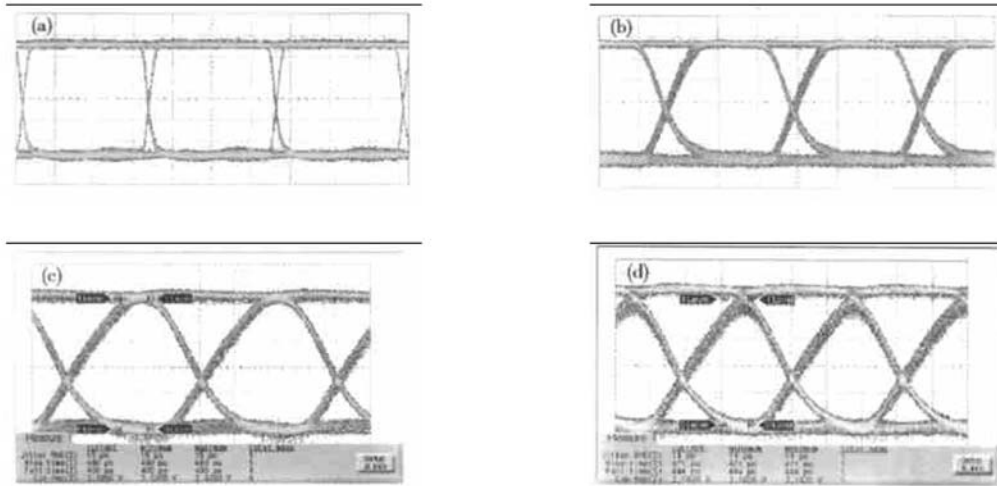


Fig. 3 (a) Output eye diagram at 155Mb/s; (b) Output eye diagram at 622Mb/s; (c) Output eye diagram at 1250Mb/s; (d) Output eye diagram at 1600Mb/s

Testing data without external DC bias on output stage are filled in Table 1. The maximum modulation voltage is over 2.36V<sub>pp</sub> corresponding with a 1.93V internal DC bias for output stage. The maximum rise time and fall time are 471ps and 360ps, respectively. And the RMS jitter is below 30ps for four bit rates. The power consumption is below 410mW under the single supply voltage of 5V.

Moreover, this driver circuit can work well with different modulation current swings under the single supply voltage ranging from 4V to 6V.

By the comparison between the simulated values and the measured values of several major parameters shown in Table 2, we can come to a con-

Table 1 Testing data without external DC bias on output stage

Data rate /(Mb·s <sup>-1</sup> )	Input signal swing/mV	Modulate voltage/V	Power dispersion < 410mW@ V <sub>DD</sub> = 5V				
			Output signal swing/V	Supply current /mA	RMS jitter /ps	t <sub>rise</sub> /ps	t <sub>fall</sub> /ps
155	500	1.93	2.36	80.30	30	400	360
622	500	1.93	2.34	80.40	13	444	367
1250	500	1.93	2.33	81.50	15	440	400
1600	500	1.93	2.18	81.75	14	471	444

Table 2 Comparison between simulated values and measured values

Parameter	Simulated value @ V <sub>DD</sub> = 5V	Measured value @ V <sub>DD</sub> = 5V
V <sub>INPUT-BUFFER</sub>	2.98V	3.0V
V <sub>REF</sub>	1.214V	1.17V
V <sub>CONT</sub>	1.997V	1.93V
V <sub>OUTPP</sub>	2.62V	2.18~ 2.36V
Supply current I <sub>DD</sub>	86mA	80.30~ 81.75mA

clusion that the performance of the fabricated chip verges on the anticipant result and can operate well at bit rates of

155, 622, and 1250Mb/s.

## 5 Conclusion

A laser diode driver for the use of optical transmitters in passive optical networks has been realized using CSMC-HJ 0.6 $\mu$ m CMOS technology. The laser driver provides a modulation current range of 0~ 50mA for an equivalent 50 $\Omega$  load. It can operate at bit rates of 155, 622, 1250, and 1600Mb/s with the rise time and fall time

of the voltage pulse falling inside the scale from 360ps to 471ps and lower RMS jitters than 30ps. The power consumption is below 410mW under a supply voltage of 5V. To sum up, this laser diode driver realized by CSMC-HJ 0.6 $\mu$ m CMOS technology can meet the requirement of 155Mb/s and 622Mb/s optical transmitters.

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## 可用于光纤用户网的 0.6 $\mu$ m CMOS 激光驱动器\*

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**摘要:** 基于国内的 CMOS 技术和 EDA 工具以及全定制的设计方法, 采用无锡华晶上华(CSMC-HJ) 0.6 $\mu$ m CMOS 技术实现了可工作于 155Mb/s、622Mb/s 的激光驱动器. 该激光驱动器在 50 $\Omega$  负载上输出电流摆幅从 0 到 50mA 可调. 在输出级 3V 直流偏置时最大输出电压摆幅可达 2.5 $V_{pp}$ . 输出电压脉冲的上升、下降时间分别小于 471ps 和 444ps. 四个工作速率下均方根抖动都小于 30ps. 电路在 5V 单电源供电时功耗小于 410mW. 芯片测试结果表明, 该激光驱动器达到了世界同类集成电路的水平.

**关键词:** 激光驱动器; CMOS; 光纤用户网

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