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Characteristics of Ultra-Thin Oxide pMOSFET Device After Soft Breakdown*

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Abstract: The degradation of MOS transistor operation due to soft breakdown of the gate oxide is studied. Important transistor parameters are monitored under homogeneous stress at different temperature until the soft breakdown occurred. The output and transfer characteristic have small change after soft breakdown as the degradations of drain current and threshold voltage is continuous. However, the increment of gate leakage current increases abruptly after the soft breakdown. The analysis to the increment of gate leakage current after the soft breakdown shows mechanism of similar Fowler-Nordheim (FN) tunneling current.

Key words: FN tunneling; MOSFET; soft breakdown; ultra-thin

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1 Introduction

Dielectric breakdown of SiO_2 is recognized as a major reliability in VSLI circuit technology. In gate oxide layers which are thinner than 5nm, soft breakdown (SBD) was observed during electrical stress of MOS devices[1]. The mechanism responsible for SBD in ultra-thin gate oxides has been investigated[2~5]. Several models have been proposed to explain the SBD I-V characteristic of an ultra-thin (T_{ox} < 5nm) gate oxide in a MOS structure. The similar Fowler-Nordheim tunneling characteristic had been shown by some researchers[4,6]. However, the above mechanism has no exact physical meaning. Lee *et al*.[1] proposed a model of its conduction mechanism. In this model, the B-mode shift is caused by the generation of the physically damaged region (PDR) at the substrate-silicon side of the oxides, which acts just as a serial resistance. At the spot, the effective thickness has become thinner and, hence, the direct tunneling that occurs is observed as the B-SILC. But it was pointed out that this model was failed to explain other characteristics of the B-SILC. The variable range hopping (VRH) conduction mechanism was proposed by Okada and Taniguchi[5]. They show that the temperature dependence of the current after soft breakdown could be quite well fit by the expression $I(T) = A\exp(-BT^{-1/4})$, for $T \in [150, 300\text{K}]$, as expected in the VRH model[7]. But they pointed out that the current behaves like a power law of the applied gate voltage after the occurrence of soft breakdown that is not consistent with the I-V characteristic of VRH ($I \propto \sinh(\beta V)$, β is a constant). Miranda and Sune *et al*. had explained the post-breakdown I-V characteristics based on the physics of mesoscopic conducting system. In this approach, the breakdown path was treated as a three dimensional quantum point contact in which

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an effective potential barrier arises as a consequence of the quantization of the transverse momentum of the passing electrons. Although they simulated the I-V characteristics in high voltage regime after soft breakdown, the characteristics of low high voltage regime was not consistent with their experiment data. And in their model, the same I-V curve could be simulated assuming different combinations of the involved parameters. Houssa *et al.*[8] also had shown that the power law behavior of the I-V characteristics of 4.2nm gate oxides can be explained by the percolation theory of nonlinear conductor networks with a distribution of percolation thresholds. However Miranda *et al.*[2] shows that a power law, for applied voltages below approximately 3.5V, and an exponential law for higher voltages are suitable fitting models. Although the above models all can explain the I-V characteristics in some ranges, the actual physical mechanism behind the SBD is still ambiguous.

In this article, the characteristics including output, transfer, and gate current of pMOSFET with 2.3nm oxide are monitored during the uniform high electric field stress. The results show that the degradations of drain current and that threshold voltage changes smoothly and continually even after the soft breakdown. But the stress induced leakage current changes abruptly when the soft breakdown occurs. And the similar Fowler-Nordheim tunneling current mechanism was observed. The percolation theory with a barrier reducing is used to explain this mechanism.

2 Results and discussion

In this study, the pMOSFETs were fabricated with gate area of $1.89\times10^{-6}cm^2$. The gate oxide thickness of 2.3nm was measured by the self-consistent quantum mechanism method[9]. HP4145B, a semiconductor parameter analyzer, was utilized to measure the current-voltage characteristics of the devices under 300, 333, 348, 363, 378, and 398K. A constant voltage source was applied to the gate in order to stress the device. The drain and source were floated to prevent the leakage passing through source of drain.

The increment ($I_{g,stress}-I_{g,origin}$) of gate leakage current, ($I_{g,stress}$ is the gate current after the voltage stress, $I_{g,origin}$ is the gate current before the voltage stress) was observed as shown in Fig. 1. The increment of gate leakage current increases gradually as SILC; then there is the discontinuous increment shown as the transition region where the increment has large change in high voltage region, and continuous change in lower voltage region; at last, when the soft breakdown occurs, the increment was discontinuous in full voltage region. But the transition region was not observed in all measured devices as shown in the inset of Fig. 1. So we took the increment shown in Fig. 1 as the leakage current after the soft breakdown.

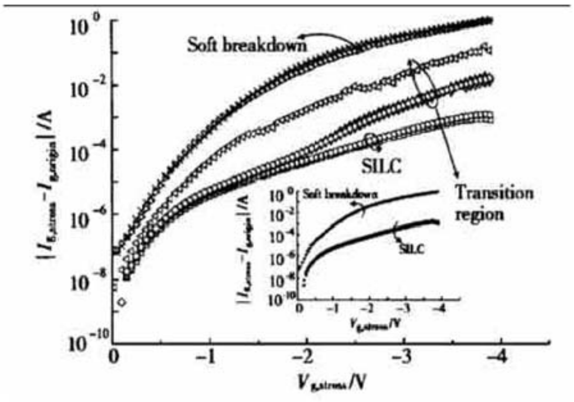

Fig. 1 Normalized increment of gate leakage current of p-MOSFET with oxide thickness 2.3nm under 90℃ per 200s stress time, $V_{g,stress}=-3.9V$, $T_{ox}=2.3nm$

Figure 2 shows that the drain current and threshold voltage change with the stress time. The data were obtained from the same devices in Fig. 1. The data were normalized by dividing the origin drain current and threshold voltage separately. From Fig. 2, the drain current and threshold voltage change gradually, even after the soft breakdown. This shows that the soft breakdown has no effect on the degradations of drain current and threshold voltage.

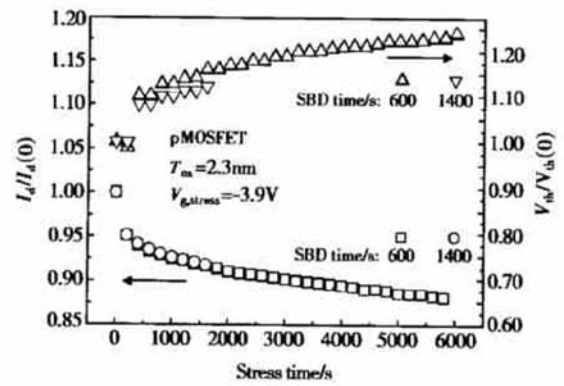

Fig. 2　Drain current and threshold voltage degradation with stress time

Figure 3 shows the behavior of gate leakage current increment, which has an abrupt increasing at some stress time thought as the soft breakdown occurring. The data were obtained from the same devices as that in the Fig. 1. The increment data of gate leakage current were normalized by dividing the maximum of gate leakage current during the range of measuring time. It is obvious the soft breakdown has great effect on gate leakage current.

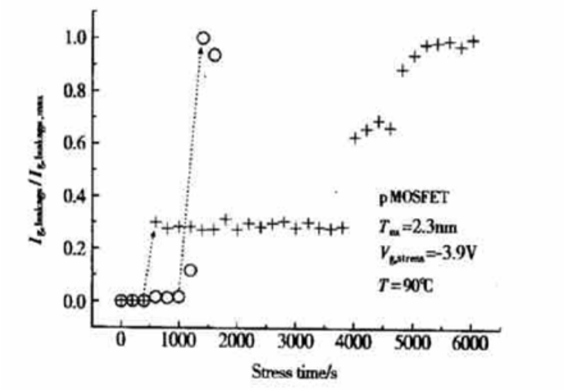

Fig. 3　Normalized gate leakage current with the stress time

For studying the mechanism of gate leakage current increment after the soft breakdown, according to different conduction processes, the experimental data dealed with are shown in Fig. 4. Table 1 gives these possible conduction processes by gate insulator layer. In Table 1, J represents the increment of gate leakage current and $F = \frac{V_g - V_{FB} - \phi_s}{T_{ox}}$, where V_{FB} is the flat band voltage,

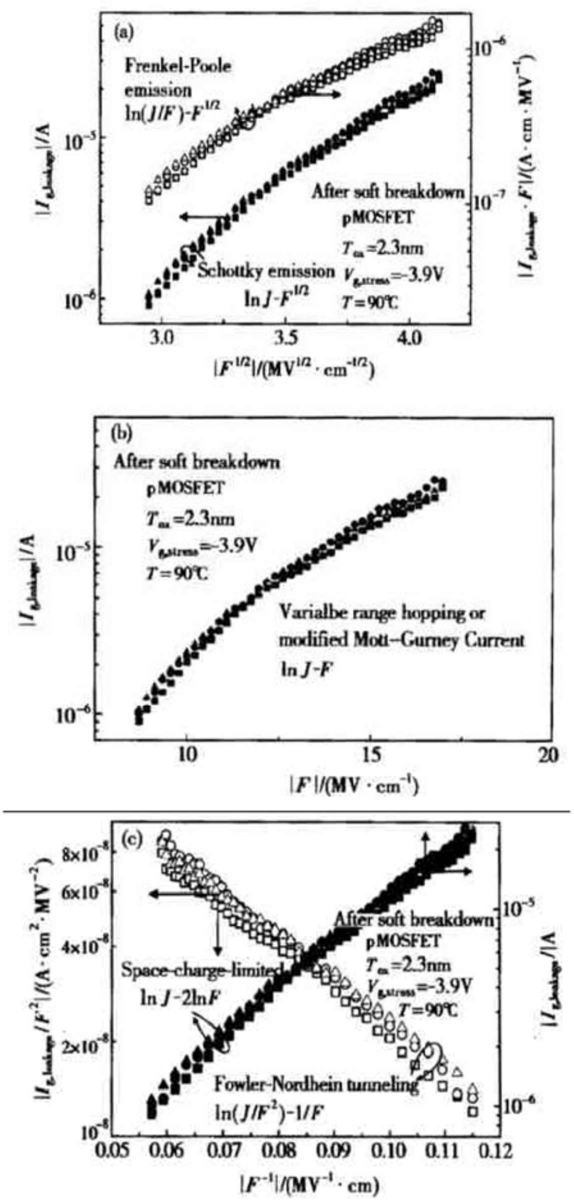

Fig. 4　Results of dealing with the experiment data according to different conduction processes　(a) Schottky emission and Frenkel-Poole emission; (b) Variable range hopping or modified Mott-Gurney current; (c) Fowler-Nordhein tunneling and Space-charge-limited current

Table 1　Possible conduction processes

Process	Format
Schottky emission[10]	$\ln J$-$F^{1/2}$
Frenkel-Poole emission[10]	$\ln(J/F)$-$F^{1/2}$
Variable range hopping[7,8]	$\ln J$-F(high electric field)
Modified Mott-Gurney current[13]	$\ln J$-F(high electric field)
Fowler-Nordhein tunneling[6]	$\ln(J/F^2)$-$1/F$
Space-charge-limited[10]	$\ln J$-$2\ln F$
Power law[8]	$\ln J$-$\gamma\ln F$

ϕ_s is the surface potential of substrate, T_{ox} is the oxide thickness, γ represents a constant. In Fig. 4, the increment of gate leakage current after the soft breakdown scans the gate voltage from −2V to −3.9V. From these curves, the relationship between $\ln(I_{g,leakage}/F^2)$ ($I_{g,leakage}$ represents the increment of gate leakage current) and $1/F$, and between $\ln(I_{g,leakage})$ and F is basically linear. This shows the FN tunneling, the space-charge-limited current or a power law may be the mechanism of making the gate leakage current to increase. Which is the mechanism to arise the gate leakage current increasing? From Ref. [10], we know when the conduction process is the space-charge-limited, the slope of curve of $\ln J$-F is 2. But this slope extracted from our experiment data is about 4.4~4.6. This shows the space-charge-limited is not the mechanism to arise the gate leakage current increasing. In addition, in Ref. [7], the authors used the percolation theory of nonlinear conductor networks with a distribution of percolation thresholds to explain the power law with the γ value about 3.1 ± 0.2. It is obvious γ value obtained in our study is different from that in Ref. [7]. So we think that the FN tunneling is mechanism of gate leakage current increment. We know the FN tunneling of SBD maybe due to the oxide thickness reduction and the barrier height reduction. Assuming the SBD gives rise to oxide thickness reduction, we know the barrier height of Si/SiO_2 is 3.15eV, so the voltage range of FN tunneling must be higher than 3.15V. However, in our experiment, we got the FN tunneling relationship between −2V and −3.9V. So we think that the soft breakdown gives rise to reduce the barrier of carrier tunneling. The standard FN expression is

$$J_{FN} = AF^2\exp(-B/F) \tag{1}$$

$$B = \frac{4}{3} \times \frac{(2m_{ox})^{1/2}}{q\hbar}\varphi_0^{3/2} \tag{2}$$

where A is a constant, φ_0 is the barrier height of electron tunneling, m_{ox} is the effective mass of oxide. From Fig. 4(c), we know the slope B can be obtained from experiment data. After obtaining the slope B using Eq. (2), we can obtain the barrier height φ_0. Figure 5 shows the barrier extracted from the gate leakage current increment after soft breakdown. This figure shows the barrier is between 0.6eV and 1.2eV, and decreases with the temperature increasing. The hollow square symbol is the average value at every temperature.

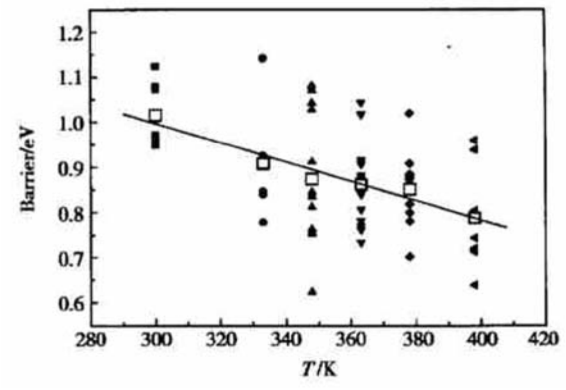

Fig. 5 Barrier extracted from the experiment at different temperature

Degraeve *et al.* [11] proposed a model to predict the statistical characteristics of breakdown events using a percolation concept, and they successfully reproduced the experimental cumulative failure (Weibull) curves of conventional oxide films. When the soft breakdown occurs, the percolation path is formed by the defects generated during the voltage stress. We think that the local property of dioxide silicon has been changed when the defects form the percolation path. That makes the barrier of Si/SiO_2 decrease. In Ref. [12], the calculation shows the gap band changes gradually from the silica gap band to silicon gap band in the interface of SiO_2/Si. We think the local defect path makes the ration of silicon and oxide in local range. This is the reason of making the barrier reduction.

3 Conclusion

In this paper, we show the soft breakdown has no effect on the degradation of drain current and threshold voltage, but great effect on the gate leakage current. After the soft breakdown, the increment of gate leakage current has the similar Fowler-Nordheim tunneling current form. It is thought that the percolation defect path arises the barrier reducing.

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超薄栅氧化物 pMOSFET 器件在软击穿后的特性*

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摘要: 研究了在软击穿后 MOS 晶体管特性的退化. 在晶体管上加均匀的电压应力直到软击穿发生的过程中监控晶体管的参数. 在软击穿后, 输出特性和转移特性只有小的改变. 在软击穿发生时, 漏端的电流和域值电压的退化是连续变化的. 但是, 在软击穿时栅漏电流突然有大量的增加. 对软击穿后的栅漏电流增量的分析表明, 软击穿后的电流机制是 FN 隧穿, 这是软击穿引起的氧化物的势垒高度降低造成的.

关键词: FN 隧穿; MOSFET; 软击穿; 超薄

PACC: 7340G; 7340Q; 7750

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