Influence of Interconnection Configuration on Thermal Dissipation of ULSI Interconnect Systems *

Xiao Xia[1,†], Yao Suying[1], and Ruan Gang[2]

(1 Center of ASIC, School of Electronic and Information Engineering, Tianjin University, Tianjin 300072, China)
(2 School of Information Science and Engineering, Fudan University, Shanghai 200433, China)

Abstract: The effects of adjacent metal layers and space between metal lines on the temperature rise of multilevel ULSI interconnect lines are investigated by modeling a three-layer interconnect. The heat dissipation of various metallization technologies concerning the metal and low-k dielectric employment is simulated in detail. The Joule heat generated in the interconnect is transferred mainly through the metal lines in each metal layer and through the path with the smallest thermal resistance in each Ield layer. The temperature rises of Al metallization are approximately ρ_{Al}/ρ_{Cu} times higher than those of Cu metallization under the same conditions. In addition, a thermal problem in 0.13μm globe interconnects is studied for the worst case, in which there are no metal lines in the lower interconnect layers. Several types of dummy metal heat sinks are investigated and compared with regard to thermal efficiency, influence on parasitic capacitance, and optimal application by combined thermal and electrical simulation.

Key words: ULSI interconnect; heat dissipation; geometrical configuration
EEACC: 2570; 2800
CLC number: TN405.97 **Document code:** A **Article ID:** 0253-4177(2006)03-0516-08

1 Introduction

In advanced ULSI interconnection systems, low dielectric constant materials are adopted to mitigate parasitic effects such as capacitance, time delay, and cross talk noise. As a major by-effect, the problem of heat dissipation becomes more critical since the thermal conductivity of low dielectric constant material is normally very low[1]. For instance, nanoporous silica (aerogel or xerogel, depending on the fabricating process) is a good candidate for insulators since its effective dielectric constant can achieve an expected value below 2[2]. However, low thermal conductivity causes serious heat transfer problems in ULSI circuits. The heat generated by current propagation along metal lines (Joule heat) must be dissipated across the dielectric films into the substrate to avoid the deterioration of the device performance and premature device failure. Thus, thermal behavior in modern ULSI interconnect systems must be taken into account. Therefore, analysis of the heat dissipation in the metallization system is very significant.

Shieh *et al*.[3] simulated the temperature distribution of a five metal layer interconnect structure with different dielectric configurations (SiO_2, low dielectric constant material, and air gaps). Chiang *et al*. investigated the effect of via separation and low-*k* dielectric materials on the thermal characteristics of multilevel VLSI Cu interconnects[4,5]. Chen *et al*. simulated the temperature rise of a power line to the substrate of the interconnection in the three cases of a single power line, a power line with a parallel signal line in the same metal layer, and a power line with an orthogonal line array in the lower metal layer[6]. We proposed heat sinks to improve heat transport in modern interconnection systems[7]. We also simulated the thermal performance of a five-multilayer ULSI interconnect[8] and deduced a set of compact quasi-analytic equations for estimating the temperature distribution of various ULSI interconnection struc-

* Project supported by the Scientific Research Foundation for Returned Overseas Chinese Scholars of the Education Ministry of China
† Corresponding author. Email: xiaxiao@tju.edu.cn; xiax58@yahoo.com
Received 13 June 2005, revised manuscript received 6 November 2005

tures[9].

There are many factors that affect thermal distribution and heat transfer in metallization interconnection systems, such as the thermal conductivity of the dielectric materials, resistivity of the metal lines, current density of the metal lines, and geometric parameters of the metallization system. Many researchers have studied the thermal behavior of interconnects with structures whose geometric parameters are fixed. However, the configuration of a multilevel interconnection may greatly affect the heat dissipation of the system. Therefore, it is important to plan carefully the interconnect configuration. Generally, the heat dissipation of a multilevel interconnection can be studied in a simplified structure. In this paper, a three-layer metallization interconnect is modeled to investigate the influence on thermal dissipation of adjacent metal layers, space between metal lines, thermal conductivity of the inter-layer dielectric (Ield) and intra-layer dielectric (Iald), and power supply. Al and Cu metallizations with various interconnect cases are studied in detail. The traditional dielectric SiO_2 and the low dielectric constant material aerogel are applied in simulation of both Cu and Al metallization. In addition, a thermal problem in 0.13μm globe interconnects is studied for the worst case, in which there are no metal lines in the lower interconnect layers. Several types of dummy metal heat sinks are investigated and compared with regard to thermal efficiency, influence on parasitic capacitance, and optimal application by combined thermal and electrical simulation.

2 Simulation of thermal dissipation

In heat transfer, the thermal energy of matter in one region is transferred to matter in another region. The thermal analysis of a system is based on the energy balance law. In this mechanism, molecular collisions cause thermal energy to be transferred from one molecule to another. Very energetic molecules lose energy in the transfer process, and lower energy molecules receive energy. The only motion is at the molecular level[10]. Heat can be conducted through a stationary solid. The temperature at any location in the system can be found by solving the heat conduction equation:

$$\frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right) + \dot{q} = \rho C_p \frac{\partial T}{\partial t} \quad (1)$$

where T is the temperature, $\dot{q}$ is the heat generation rate, ρ is the density, C_p is the heat capacity, t is the time, and k_x, k_y, k_z are the thermal conductivities in the x, y, and z directions, respectively. For static heat transfer, T is independent of t.

In an interconnect, the Joule heat generated by current in the metal lines should dissipate easily into the substrate to avoid limitations of device performance and premature device failure. The heat generation rate $\dot{q}$ of the metal lines can be calculated by

$$\dot{q} = \frac{I^2 Rt}{tV} = (JA)^2 \rho_{metal} \frac{l}{A} \times \frac{1}{lA} = J^2 \rho_{metal} \quad (2)$$

where V is the volume, I is the current, R is the resistance of the metal line, J is the current density, ρ_{metal} is the metal resistivity, and l and A are the length and area of the metal line, respectively.

Figure 1 shows a cross section of the simulated interconnection, in which M and S are the distances between the two metal lines in the first metal layer and the second metal layer, respectively. The temperature distribution of the interconnects depends on geometric parameters, resistivity of the metal, thermal conductivity of the dielectrics, and power supply. The main objective of this study is to investigate the influences of adjacent metal layers and the distance between the metal lines on the heat dissipation. It is assumed that heat flows only downward to the silicon substrate, which is usually attached to a heat sink.

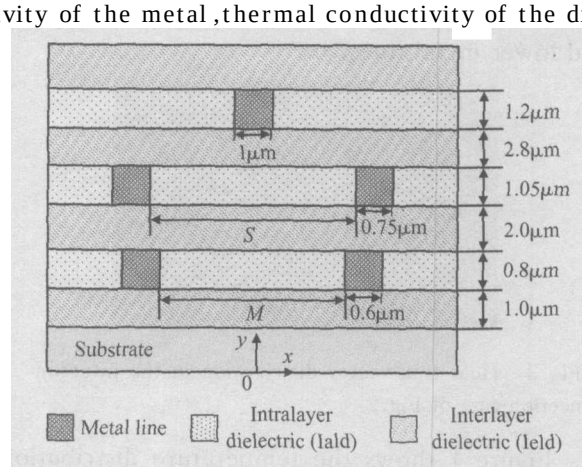

Fig. 1　Schematic cross section of the simulated interconnection structure

The finite element software ANSYS is applied to simulate the thermal dissipation. Figure 2 shows the temperature distribution on a three-metal-layer Cu metallization system. Here, the current propagates only through the top metal line. The dielectric insertion case is SiO_2/aerogel (Ield/Iald). In this study, the substrate temperature is

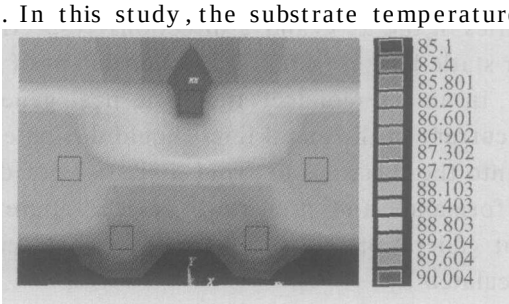

Fig. 2 Temperature distribution (in ℃) of a three-metal-layer Cu interconnect structure (the Ield is SiO_2 and the Iald is aerogel)

set at 85 ℃. The thermal conductivities of SiO_2, the aerogel applied for the Ield, and the aerogel applied for the Iald are 1.0, 0.010[11], and 0.065 W/mK[12], respectively. Figure 3 shows the corresponding heat flux vector distribution in this structure. It is obvious that the heat transfers mainly through the metal lines in each metal layer, and through the path with the smallest L/k (the order of the thermal resistance) in each Ield layer, where L is the distance between the upper and lower metal lines.

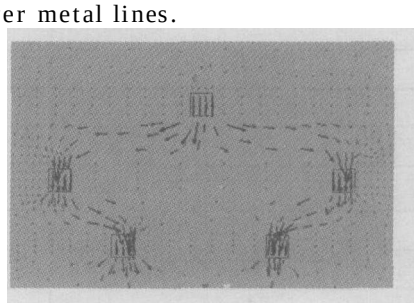

Fig. 3 Heat flux vector distribution in the interconnection case of Fig. 2

Figure 4 shows the temperature distribution at different locations on the path of x = 0 of the interconnection system shown in Fig. 1. T_1, T_2, T_3, and T_4 are the interconnect system temperatures for the material insertion cases: (1) as depicted in Fig. 1; (2) the second metal layer is completely occupied by aerogel, i. e., there are no metal lines in this layer; (3) the first and second metal layers are completely occupied by aerogel; and (4) the first metal layer is completely occupied by aerogel. The curves indicate that the main thermal resistance comes from the aerogel layer. One aerogel layer leads to a temperature increase of about 10 ℃ in this structure. The thermal resistance of SiO_2 film is about two orders of magnitude smaller than that of aerogel film of the same thickness. Therefore, suitably designed metal insertions in the dielectric layers, especially in the aerogel layers, are desired for the heat dissipation.

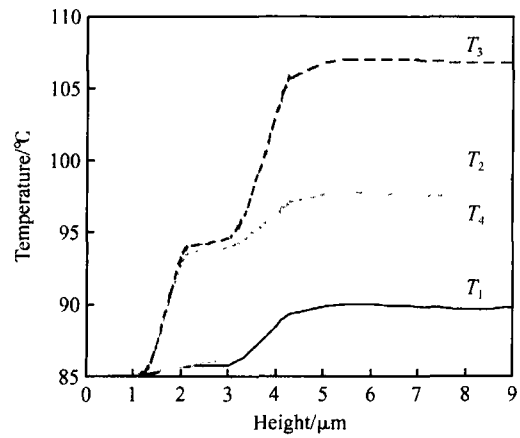

Fig. 4 Temperature distribution of the three-metal-layer Cu interconnect structure at x = 0 (refer to Fig. 1) for various technologies

Figures 5～7 show the temperature rises from the substrate to the top metal line for the interconnect structure of Fig. 1. Various kinds of metallization technologies are simulated to investigate the effects of different factors (such as geometric configurations, current density, metal and dielectric employment, and power applications) on the heat dissipation of interconnection systems.

These studies indicate that temperature rise varies for different interconnect technologies. The temperature rises in Fig. 5 are from the substrate to the top metal line for the dielectric employment of SiO_2/aerogel (Ield/Iald) for Al and Cu metallization. The temperature rises of Al metallization are approximately ρ_{Al}/ρ_{Cu} times higher than those of Cu metallization under the same conditions. It is found that the second metal layer is more critical than the first for heat dissipation. For the (c) and (d) cases, the temperature rise increases first with the decrease of 1/S but suffers a decrease when 1/S = 0, corresponding to the case in which there is no metal line in the layer. This is because there is no heat source in this layer, and

the heat generated in the first metal layer is easily conducted to the substrate through the SiO_2 film underneath. Temperature rise increases continuously with the decrease of 1/ M. Even though there is no heat source in this layer in the case of 1/ M = 0, it is more difficult for the Joule heat generated above to dissipate into the substrate.

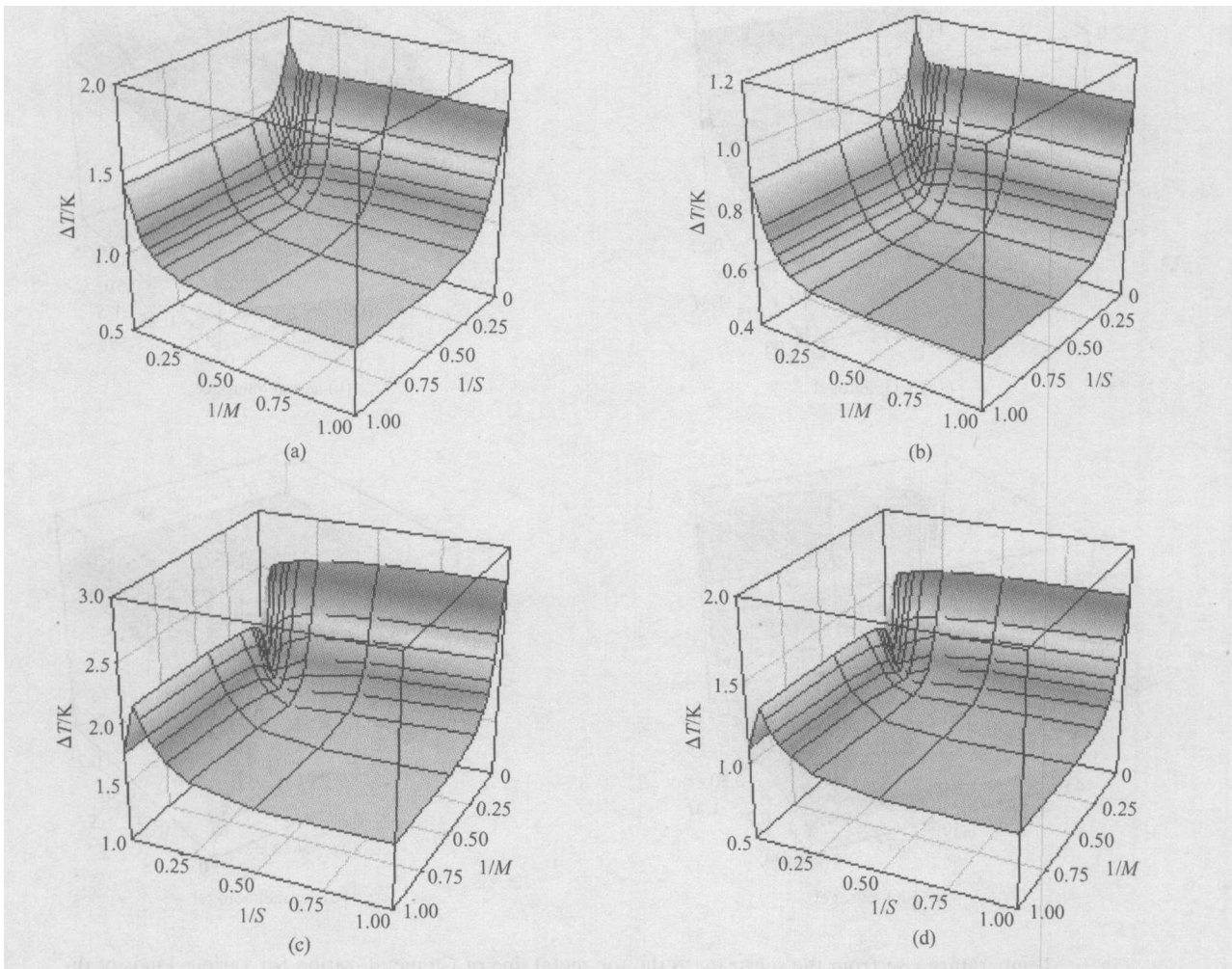

Fig. 5　Temperature rises from the substrate to the top metal line for dielectric configuration of SiO_2/ aerogel (Ield/ Iald) for Al and Cu metallization with J = 0. 5MA/ cm^2　(a) Al, current through the top metal line; (b) Cu, current through the top metal line; (c) Al, current through all metal lines; (d) Cu, current through all metal lines

Figure 6 presents temperature rises from the substrate to the top metal line of Cu metallization for various dielectrics employed for Ield/ Iald. For the same situation, temperature rise is proportional to J^2. It is found that temperature rises for the dielectric Ield/ Iald cases of SiO_2/ aerogel and aerogel/ aerogel are very different. Temperature rises are lower when metal lines are located close to each other in the case of SiO_2/ aerogel but higher in the case of aerogel/ aerogel. When aerogel is employed as Ield, it is difficult for the Joule heat to be conducted to the substrate due to the ultra low thermal conductivity of the aerogel. There is much more Joule heat generated per volume when the metal lines are near than when they are far. Therefore, the temperature rise decreases with the increase of S and M. However, the behavior of temperature rises is reversed when SiO_2 is employed as Ield because the generated Joule heat is easily conducted to the substrate through the SiO_2 film.

Figure 7 gives temperature rises from the substrate to the top metal line of Cu metallization for various dielectrics employed for Ield/ Iald. Tem-

perature rises for the Ield/ Iald dielectric configuration aerogel/ aerogel are approximately $k_{SiO_2}/k_{aerogel}$ times higher than those in the SiO_2/ aerogel or SiO_2/SiO_2 configurations.

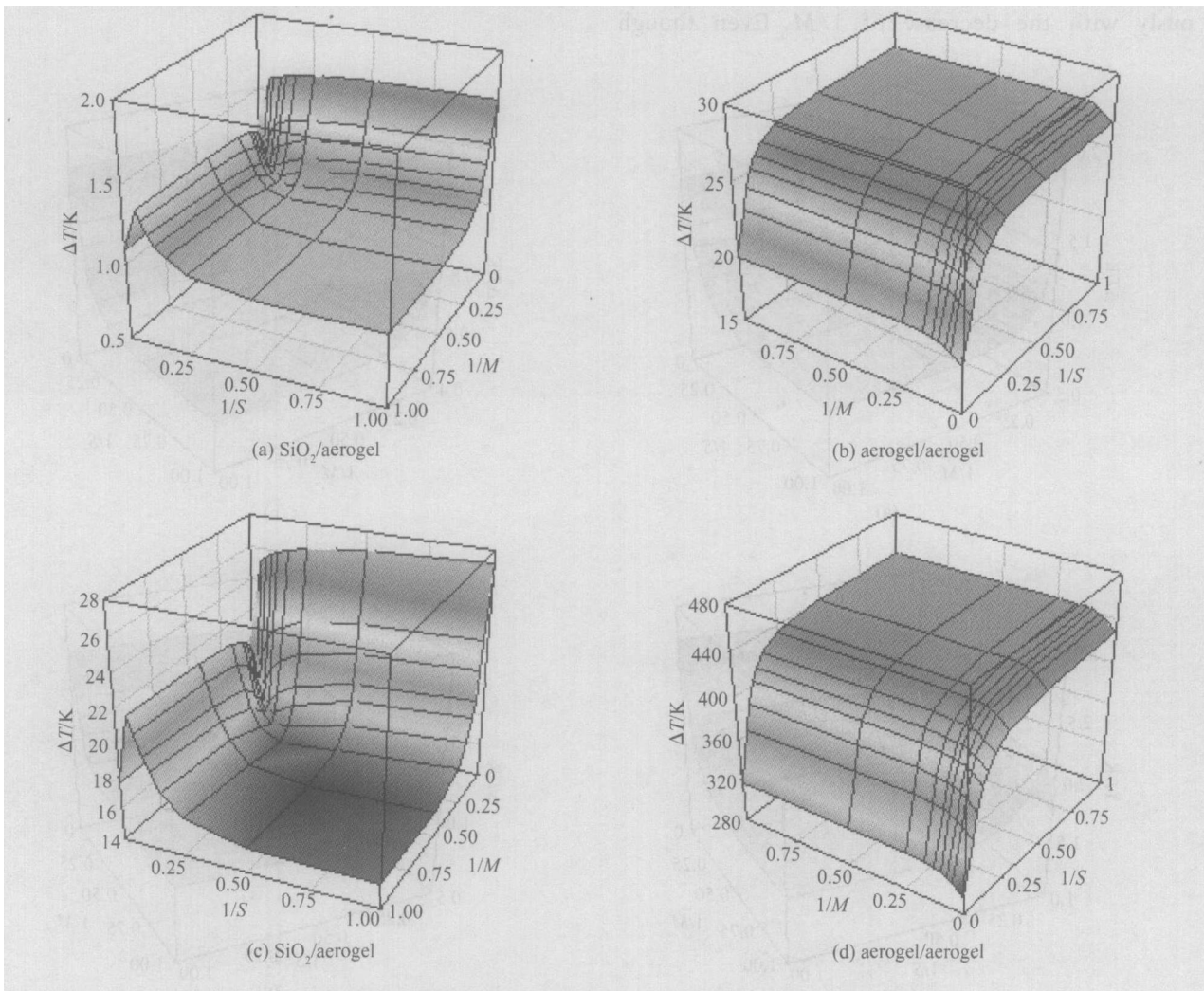

Fig. 6 Temperature rise from the substrate to the top metal line of Cu metallization for various kinds of dielectric employment of Ield/ Iald Here the current propagates through all metal lines with J = 0.5(a, b) and 2MA/ cm^2 (c, d), respectively.

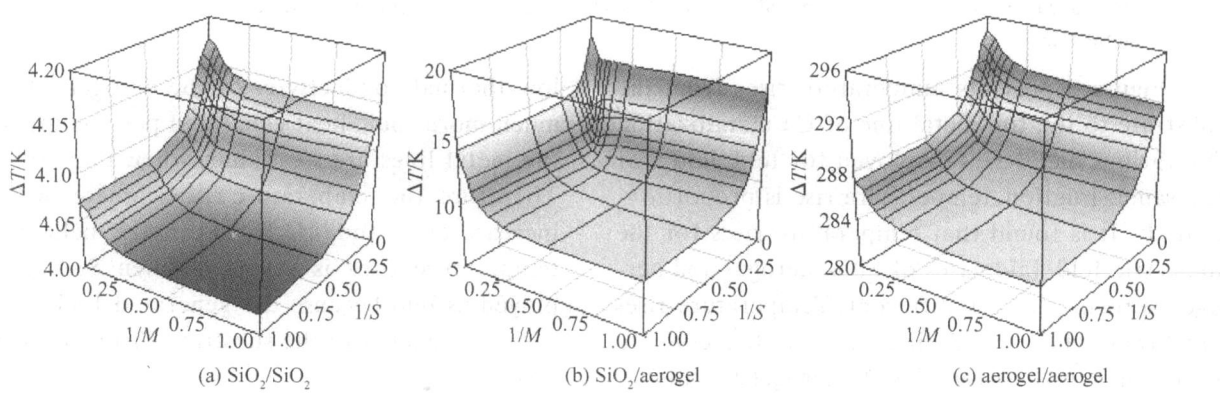

Fig. 7 Temperature rises from the substrate to the top metal line of Cu metallization for various kinds of dielectric employment for Ield/ Iald Here the current propagates only through the top metal line with J = 2MA/ cm^2.

The above simulation indicates that heat dissipation is a crucial aspect of ULSI interconnects. This thermal problem is more critical for higher technology node ICs since they have much more interconnect layers and are inevitably employed with low-k materials. The simulated results show that the vital thermal problem occurs in the cases in which there are no metals under the signal line, corresponding to 1/ M = 0, 1/ S = 0, and so on. Such a situation might be the globe signal line between function blocks[7]. To understand the heat dissipation in high technology node ICs, the globe line in the case with no metal lines underneath is investigated for a 0.13μm ULSI interconnection. The adopted geometric parameters of the interconnection are the results of an electrical multi-objective optimization[13]. In the structure, the globe line is located in the 6th metal layer. Figure 8 shows the temperature rises in the globe line for different dielectrics: (A) homogeneously inserted aerogel; (B) embedded aerogel; (C) homogeneously inserted polymer low-*k* material; and (D) dense SiO_2. The gray bands cover the range of substrate temperature, which is assumed to be from 80 (lower bound) to 150 ℃(upper bound). Four situations, a, b, c, and d, stand for aerogel/ aerogel, SiO_2/ aerogel, polymer/ polymer, and SiO_2/ SiO_2 employed as the Ield/ Iald, respectively. The thermal conductivity for polymer low-*k* is around 0.25W/ mK. In the figure, the *x*-axis parameter of thermal conductance per unit line length between the heated metal line and the substrate is proportional to the thermal conductivity of the medium on the heat transfer path and the cross section through which the heat flows, and inversely proportional to the length of the heat transfer path[14].

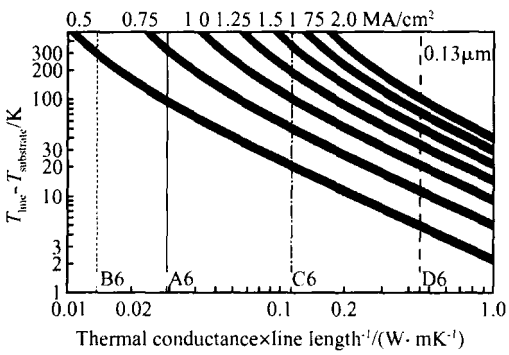

Fig. 8　Temperature rises on the globe line (in the 6th metal layer for 0.13μm generation) in the case without metal lines in the lower metal layers for different dielectric configuration　(A) Homogeneously inserted aerogel; (B) Embedded aerogel; (C) Homogeneously inserted polymer low-k material; (D) Dense SiO_2

Compared to the worst case discussed above for a long global line with no locally occupied lower metal layers, the actual temperature of the global interconnects can be locally reduced by high metal densities in the lower levels or by dummy metal lines which can reduce the thermal resistance between the global lines and the substrate. The temperature increase above the densely metal-packed area is found to be several degrees. Thus, the globe line temperature above the unoccupied area depends on the span distance between the densely packed functional blocks, as shown in Fig. 9. The results indicate that a long span and poor thermal conductivity of the materials cause this vital thermal problem in such globe interconnects.

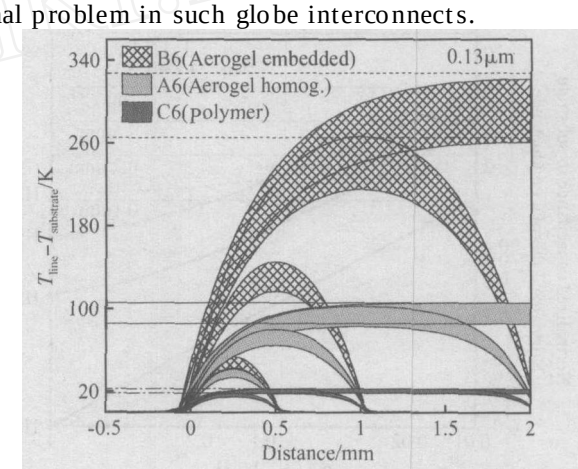

Fig. 9　Temperature distribution along the global lines above unoccupied lower metal layers between function blocks of 0.5, 1, 2, and 4mm distance for 0.5MA/ cm²

To improve heat transport from global interconnects downward through the less occupied lower metal layers, additional dummy metal lines (metal plugs consisting of W in level M1 and of Cu in the higher levels, depending on the technology) acting as heat sinks can be placed. However, dummy metals simultaneously increase the *RC* constant since they increase the capacitance. The optimal configuration and distribution of dummy lines should be determined by a combined thermal and electrical calculation. Three kinds of heat sinks depicted in Fig. 10 have been investigated with regard to their thermal efficiency and to their influence on the parasitic line to ground capacitance. Figure 11

demonstrates the resulting impact of dummy heat sink insertion on the thermal conductance and capacitance between global interconnects and substrate for different properties of the dielectrics. Special values of conductivity and dielectric constants are marked on the top edge of the frame, respectively. A dielectric constant of 1.3 corresponds to a 0.01W/mK dielectric and 1.8 to 0.065 W/mK[7]. To calculate the thermal conductance and capacitance of a cooled interconnect, the respective values of the uncooled line and the additional contributions of the heat sinks in Fig. 11 have to be added. In the case of the homogeneous insertion scheme, conductance and capacitance are increased by the same factor. For the embedded insertion of an aerogel, however, (e.g. $\lambda_{ald}/\lambda_{eld} = 0.01/1$, $\varepsilon_{ald}/\varepsilon_{eld} = 1.3/4.1$) the thermal conductance of a 100μm long segment of a global interconnect, cooled by one heat sink of type HS1, is increased 4.6 times, whereas its capacitance is increased only by a factor of 1.24. The study finds more effective cooling of the same line segment by heat sink HS2 (thermal conductance is increased 10.2 times) would increase parasitic capacitance by 1.7, which is unacceptable. Otherwise, HS2 is efficient for the cooling of long interconnects. Furthermore, the resistivity of metal increases with the temperature rise and can be approximated by $\rho_T = \rho_{ref}(1 + \alpha_T(T - T_{ref}))$. Here ρ_T and ρ_{ref} are the metal resistivities at temperature T and reference temperature T_{ref}, respectively. The coefficient α_T is the temperature coefficient of resistivity. For Cu, α_T is around 0.004/℃, which means the resistance of Cu will be increased by around 1.4 if the temperature increases by 100 ℃. Therefore, keeping the temperature of the metal line low is also important to prevent the increase of the RC time delay. A proper heat sink designed at the key location of the interconnection system is necessary to avoid undesired thermal effects such as electron migration in the metal line and degradation of the chip. According to the above study, the effective cooling of global interconnects depends on line length and should be adjusted by a combined thermal and electrical design.

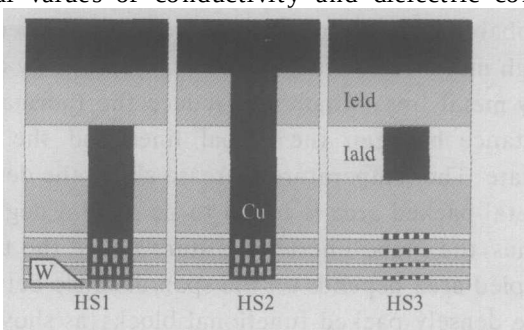

Fig. 10 Different types of dummy heat sinks for cooling global interconnects

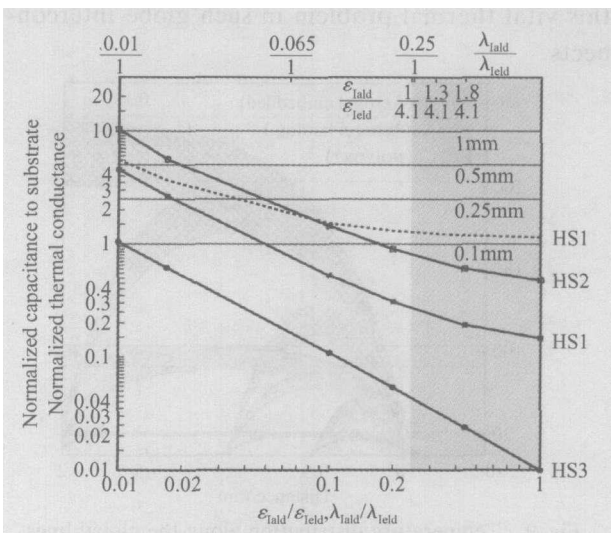

Fig. 11 Dependence of normalized thermal conductance (solid line) and capacitance (dashed line) on the ratio of thermal conductivity and dielectric constants for different types of dummy heat sinks, respectively The quantities are normalized to the corresponding values of a 100μm long uncooled interconnect of level M6 (0.13μm). Horizontal lines refer to uncooled interconnects of different lengths.

3 Conclusion

Interconnection configurations and metal line geometry have a strong influence on the heat transfer capability of interconnection systems. Therefore, very careful planning of the interconnect configuration is necessary. The results obtained here can be applied to qualitatively estimate the thermal dissipation of the similar structures.

The electrical resistivities and thermal conductivities of Cu and Al, as well as the thermal conductivities of SiO_2 and aerogel, are crucial factors in the heat dissipation in a ULSI interconnection at a certain power level. When aerogel is employed as Ield, the thermal problems of interconnection systems are critical due to the ultra low thermal conductivity of aerogel. It is found that temperature ri-

ses for the dielectric Ield/ Iald configuration of aerogel/ aerogel are approximately $k_{SiO_2}/k_{aerogel}$ times higher than those in the case of SiO_2/ aerogel or SiO_2/ SiO_2.

Longer vertical distances from the upper line to the substrate and poor thermal conductivity of the dielectrics inhibit the dissipation of heat to the substrate. This situation will be much more serious for a global line above locally unoccupied metal layers, as in the case of global lines between function blocks. The insertion of dummy heat sinks is an appropriate means to restrain interconnect temperatures. Various types of the heat sinks differ with regard to their thermal efficiency and to their contribution to parasitic capacitance. The optimal choice and placement of the different types depend on the properties of the dielectrics and on the individual interconnect length. The combined electrical and thermal optimization of the interconnect cooling is becoming more important for future ULSI interconnection design.

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超大规模集成电路互连系统的布线构造对散热的影响*

肖　夏[1,†]　姚素英[1]　阮　刚[2]

(1 天津大学电子信息工程学院 专用集成电路设计中心，天津　300072)

(2 复旦大学信息科学与工程学院，上海　200433)

摘要：应用一个三层互连布线结构研究了诸多因素尤其是布线的几何构造对互连系统散热问题的影响，并对多种不同金属与介质相结合的互连布线的散热情况进行了详细模拟. 研究表明互连线上焦耳热的主要散热途径为金属层内的金属线和介质层中热阻相对小的路径. 因此互连系统的几何布线对系统散热具有重要影响. 在相同条件下，铝布线系统的温升约为铜布线的ρ_{Al}/ρ_{Cu}倍. 此外，模拟了 0.13μm 工艺互连结构中连接功能块区域的信号线上的温升情况，探讨了几种用于改善热问题的散热金属条对互连布线的导热和附加电容的影响.

关键词：ULSI 互连布线；散热；几何构造

EEACC：2570；2800

中图分类号：TN405.97　　**文献标识码**：A　　**文章编号**：0253-4177(2006)03-0516-08

*教育部留学归国基金资助项目

†通信作者. Email: xiaxiao@tju.edu.cn; xiax58@yahoo.com

2005-06-13 收到，2005-11-06 定稿